24LC024/24LC025

2K 2.5V I^{2}C™ Serial EEPROM

FEATURES

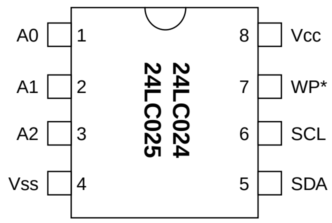
- Single supply with operation from 2.5 to 5.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
- Organized as a single block of 128 bytes (256 x 8)
- Hardware write protection for entire array (24LC024)
- 2-wire serial interface bus, I^{2}C compatible
- 100kHz and 400kHz compatibility
- Page-write buffer for up to 16 bytes
- Self-timed write cycle (including auto-erase)
- 3.5 ms typical write cycle time for page write
- Address lines allow up to eight devices on bus
- 10,000,000 erase/write cycles guaranteed
- ESD protection > 4,000V
- Data retention > 200 years
- 8-pin PDIP, SOIC or TSSOP packages
- Available for extended temperature ranges
  - Commercial (C): 0°C to +70°C
  - Industrial (I): -40°C to +85°C

DESCRIPTION

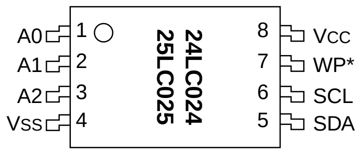
The Microchip Technology Inc. 24LC024/24LC025 is a 2K bit Serial Electrically Erasable PROM with a voltage range of 2.5V to 5.5V. The device is organized as a single block of 256 x 8-bit memory with a 2-wire serial interface. Low current design permits operation with typical standby and active currents of only 10 µA and 1 mA respectively. The device has a page-write capability for up to 16 bytes of data. Functional address lines allow the connection of up to eight 24LC024/24LC025 devices on the same bus for up to 16K bits of contiguous EEPROM memory. The device is available in the standard 8-pin PDIP, 8-pin SOIC (150 mil), and TSSOP packages.

PACKAGE TYPES

PDIP/SOIC

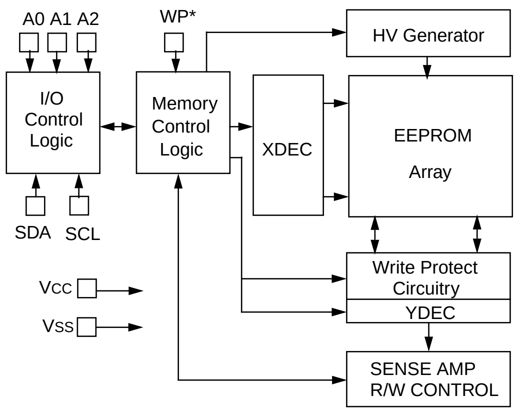


TSSOP



*WP pin available only on 24LC024. This pin has no internal connection on 24LC025

BLOCK DIAGRAM



*WP pin available only on 24LC024. This pin has no internal connection on 24LC025

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{CC} 7.0V
All inputs and outputs w.r.t. V_{SS}...... -0.6V to V_{CC} +1.0V
Storage temperature ....-65˚C to +150˚C
Ambient temp. with power applied.......-65˚C to +125˚C
Soldering temperature of leads (10 seconds) ...+300˚C
ESD protection on all pins ....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
V_{SS}	Ground
SDA	Serial Data
SCL	Serial Clock
V_{CC}	+2.5V to 5.5V Power Supply
A0, A1, A2	Chip Selects
WP	Hardware Write Protect (24LC024)
NC	No internal connection

TABLE 1-2: DC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.	V_{CC} = +2.5V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
SCL and SDA pins:					
High level input voltage	V_{IH}	0.7 V_{CC}		V	
Low level input voltage	V_{IL}		0.3 V_{CC}	V	
Hysteresis of Schmitt trigger inputs	V_{HYS}	0.05 V_{CC}	—	V	(Note)
Low level output voltage	V_{OL}		0.40	V	I_{OL} = 3.0 mA, V_{CC} = 4.5V I_{OL} = 2.1 mA, V_{CC} = 2.5V
Input leakage current	I_{LI}	-10	10	µA	V_{IN} = 0.1V to 5.5V, WP = Vss
Output leakage current	I_{LO}	-10	10	µA	V_{OUT} = 0.1V to 5.5V
Pin capacitance (all inputs/outputs)	C_{IN}, C_{OUT}	—	10	pF	V_{CC} = 5.0V (Note) Tamb = 25°C, f = 1 MHz
Operating current	I_{CC} Read	—	1	mA	V_{CC} = 5.5V, SCL = 400 kHz
	I_{CC} Write	—	3	mA	V_{CC} = 5.5V
Standby current	I_{CCS}	—	50	µA	V_{CC} = 5.5V, SDA = SCL = V_{CC} A0, A1, A2 = Vss
Note: This parameter is periodically sampled and not 100% tested.					

TABLE 1-3: AC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.	Vcc = 2.5V to 5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C

Parameter	Symbol	Vcc = 2.5V - 5.5V STD MODE		Vcc = 4.5V - 5.5V FAST MODE		Units	Remarks
		Min.	Max.	Min.	Max.		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VIL maximum	TOF	—	250	20 +0.1 C_B	250	ns	(Note 1), $C_B \leq 100$ pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWC	—	10	—	10	ms	Byte or Page mode
Endurance		10M	—	10M	—	cycles	25°C, VCC = 5.0V, Block Mode (Note 4)

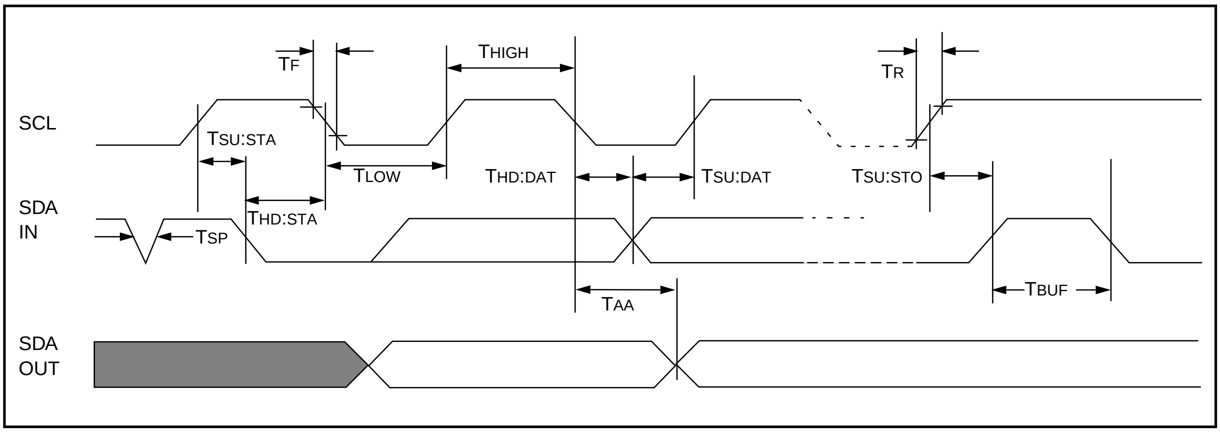
Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

FIGURE 1-1: BUS TIMING DATA



2.0 PIN DESCRIPTIONS

2.1 SDA Serial Data

This is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to V_{CC} (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

2.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

2.3 A0, A1, A2

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 24LC024/24LC025 devices may be connected to the same bus by using different chip select bit combinations. These inputs must be connected to either V_{CC} or V_{SS}.

2.4 WP (24LC024 only)

This is the hardware write protect pin. It must be tied to V_{CC} or V_{SS}. If tied to Vcc, the hardware write protection is enabled. If the WP pin is tied to Vss the hardware write protection is disabled. Note that the WP pin is available only on the 24LC024. This pin is not internally connected on the 24LC025.

2.5 Noise Protection

The 24LC024/24LC025 employs a V_{CC} threshold detector circuit which disables the internal erase/write logic if the V_{CC} is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

3.0 FUNCTIONAL DESCRIPTION

The 24LC024/24LC025 supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC024/24LC025 works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

4.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

4.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

4.5 Acknowledge

Each receiving device, when addressed, is required to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24LC024/24LC025 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition (Figure 4-2).

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS CHARACTERISTICS

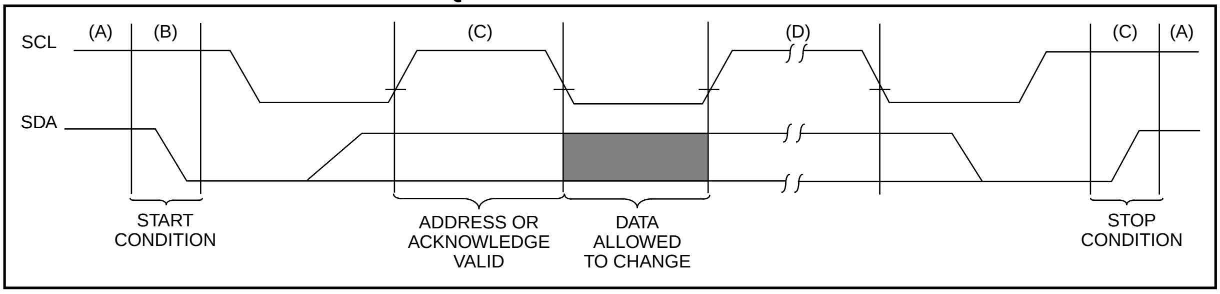
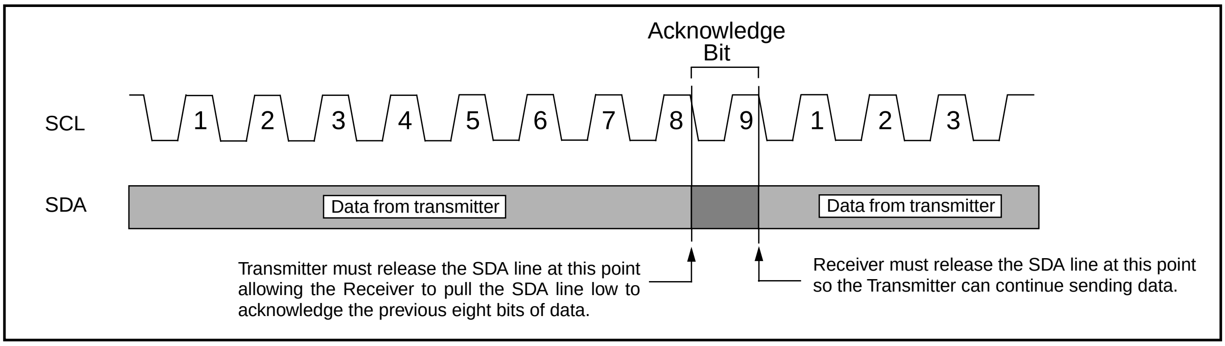


FIGURE 4-2: ACKNOWLEDGE TIMING

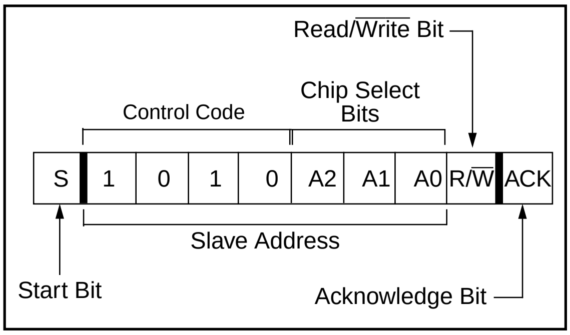


5.0 DEVICE ADDRESSING

A control byte is the first byte received following the start condition from the master device (Figure 5-1). The control byte consists of a four bit control code; for the 24LC024/24LC025 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the chip select bits (A2, A1, A0). The chip select bits allow the use of up to eight 24LC024/24LC025 devices on the same bus and are used to select which device is accessed. The chip select bits in the control byte must correspond to the logic levels on the corresponding A2, A1, and A0 pins for the device to respond. These bits are in effect the three most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. Following the start condition, the 24LC024/24LC025 monitors the SDA bus checking the control byte being transmitted. Upon receiving a 1010 code and appropriate chip select bits, the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24LC024/24LC025 will select a read or write operation.

FIGURE 5-1: CONTROL BYTE FORMAT



5.1 Contiguous Addressing Across Multiple Devices

The chip select bits A2, A1, A0 can be used to expand the contiguous address space for up to 16K bits by adding up to eight 24LC024/24LC025 devices on the same bus. In this case, software can use A0 of the control byte as address bit A8, A1 as address bit A9, and A2 as address bit A10. It is not possible to sequentially read across device boundaries.

 Preliminary

6.0 WRITE OPERATIONS

6.1 Byte Write

Following the start signal from the master, the device code(4 bits), the chip select bits (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. The device will acknowledge this control byte during the ninth clock pulse. The next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC024/24LC025. After receiving another acknowledge signal from the 24LC024/24LC025 the master device will transmit the data word to be written into the addressed memory location. The 24LC024/24LC025 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC024/24LC025 will not generate acknowledge signals (Figure 6-1). If an attempt is made to write to the protected portion of the array when the hardware write protection (24LC024 only) has been enabled, the device will acknowledge the command but no data will be written. The write cycle time must be observed even if the write protection is enabled.

6.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC024/24LC025 in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to 15 additional data bytes to the 24LC024/24LC025 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order four bits of the word address remains constant. If the master should transmit more than 16 bytes prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 6-2). If an attempt is made to write to the protected portion of the array when the hardware write protection has been enabled, the device will acknowledge the command but no data will be written. The write cycle time must be observed even if the write protection is enabled.

6.3 WRITE PROTECTION

The WP pin (available on 24LC024 only) must be tied to VCC or VSS. If tied to VCC, the entire array will be write protected. If the WP pin is tied to VSS, then write operations to all address locations are allowed.

FIGURE 6-1: BYTE WRITE

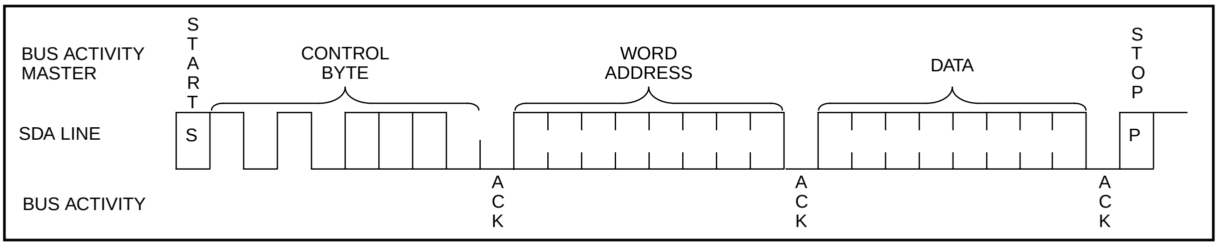
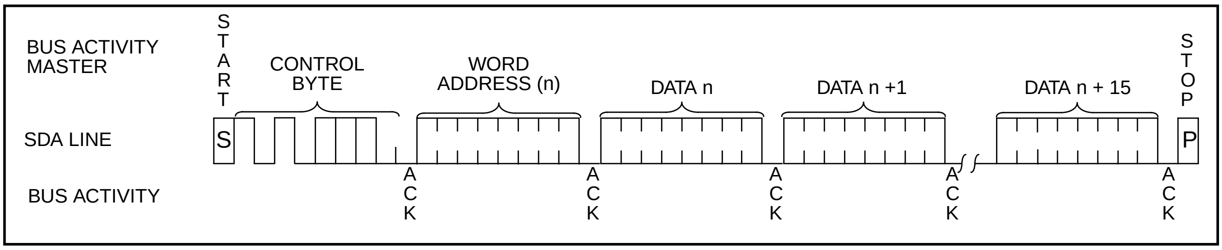


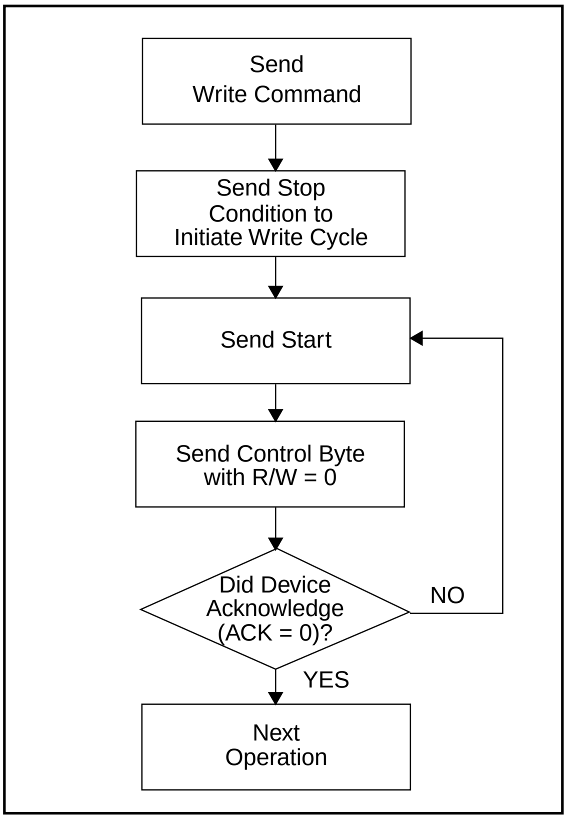
FIGURE 6-2: PAGE WRITE



7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the start bit and control byte must be re-sent. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 READ OPERATIONS

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

8.1 Current Address Read

The 24LC024/24LC025 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ bit set to one, the 24LC024/24LC025 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC024/24LC025 discontinues transmission (Figure 8-1).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC024/24LC025 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC024/24LC025 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC024/24LC025 discontinues transmission (Figure 8-2). After this command, the internal address counter will point to the address location following the one that was just read.

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC024/24LC025 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC024/24LC025 to transmit the next sequentially addressed 8-bit word (Figure 8-3).

To provide sequential reads the 24LC024/24LC025 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The internal address pointer will automatically roll over from address 0FFh to address 000h.

FIGURE 8-1: CURRENT ADDRESS READ

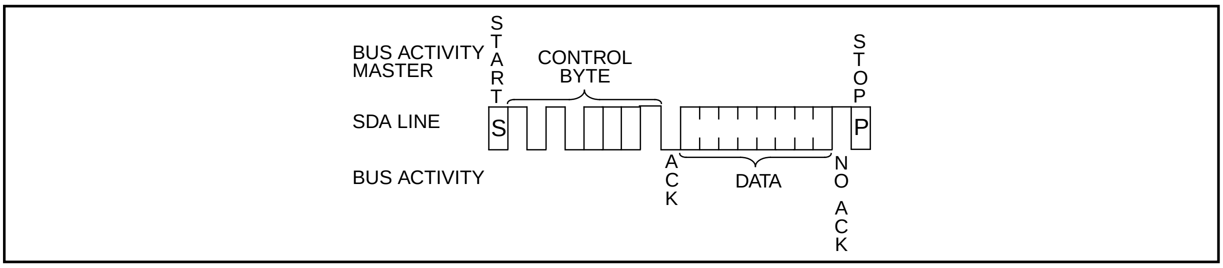


FIGURE 8-2: RANDOM READ

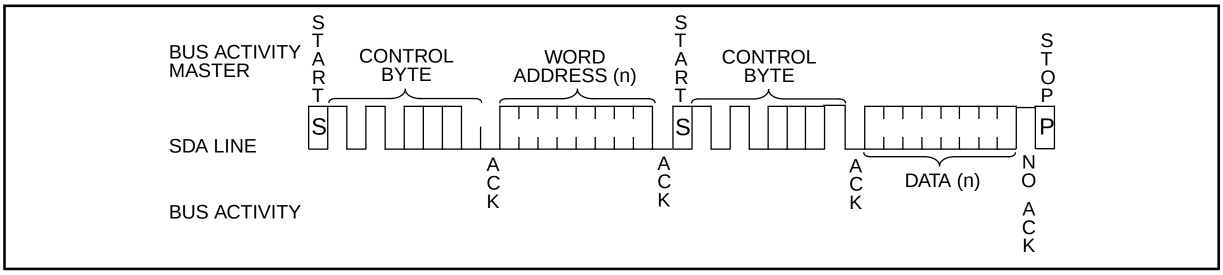
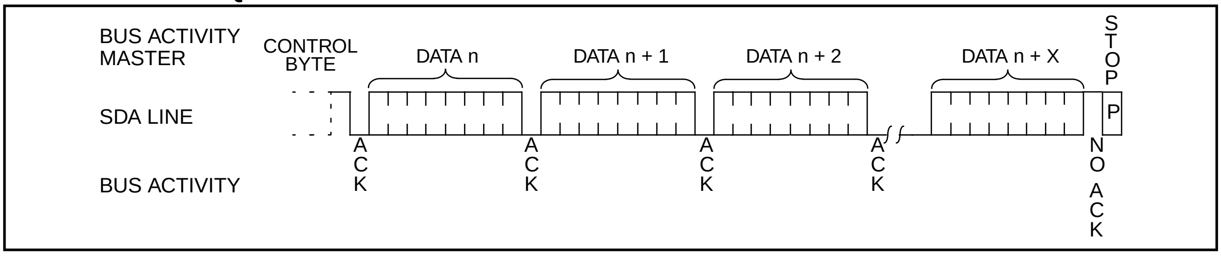


FIGURE 8-3: SEQUENTIAL READ



NOTES:

24LC024/24LC025 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

24LC024/24LC025 — _ /P

Package:	P	=	Plastic DIP (300 mil Body), 8-lead
	SN	=	Plastic SOIC (150 mil Body), 8-lead
	ST	=	TSSOP, 8-lead
Temperature Range:	Blank	=	0°C to +70°C
	I	=	–40°C to +85°C
Device:	24LC024		2K I^2C Serial EEPROM with WP
	24LC024T		2K I^2C Serial EEPROM with WP pin (Tape and Reel)
	24LC025		2K I^2C Serial EEPROM
	24LC025T		2K I^2C Serial EEPROM (Tape and Reel)

Sales and Support

Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office.
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277.
3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

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