



74LVX03

LOW VOLTAGE CMOS QUAD 2-INPUT NAND GATE (OPEN DRAIN) WITH 5V TOLERANT INPUTS

- HIGH SPEED :
 $t_{PD} = 4.8ns$ (TYP.) at $V_{CC} = 3.3V$
- 5V TOLERANT INPUTS
- INPUT VOLTAGE LEVEL :
 $V_{IL} = 0.8V$, $V_{IH} = 2V$ at $V_{CC} = 3V$
- LOW POWER DISSIPATION:
 $I_{CC} = 2 \mu A$ (MAX.) at $T_A = 25^\circ C$
- LOW NOISE:
 $V_{OLP} = 0.3V$ (TYP.) at $V_{CC} = 3.3V$
- OPERATING VOLTAGE RANGE:
 $V_{CC}(OPR) = 2V$ to $3.6V$ (1.2V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 03
- IMPROVED LATCH-UP IMMUNITY
- POWER DOWN PROTECTION ON INPUTS



ORDER CODES

PACKAGE	TUBE	T & R
SOP	74LVX03M	74LVX03MTR
TSSOP		74LVX03TTR

DESCRIPTION

The 74LVX03 is a low voltage CMOS OPEN DRAIN HEX INVERTER fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It is ideal for low power, battery operated and low noise 3.3V applications.

The internal circuit is composed of 3 stages including buffer output, which provides high noise immunity and stable output.

This device can, with an external pull-up resistor, be used in wired AND configuration. This device

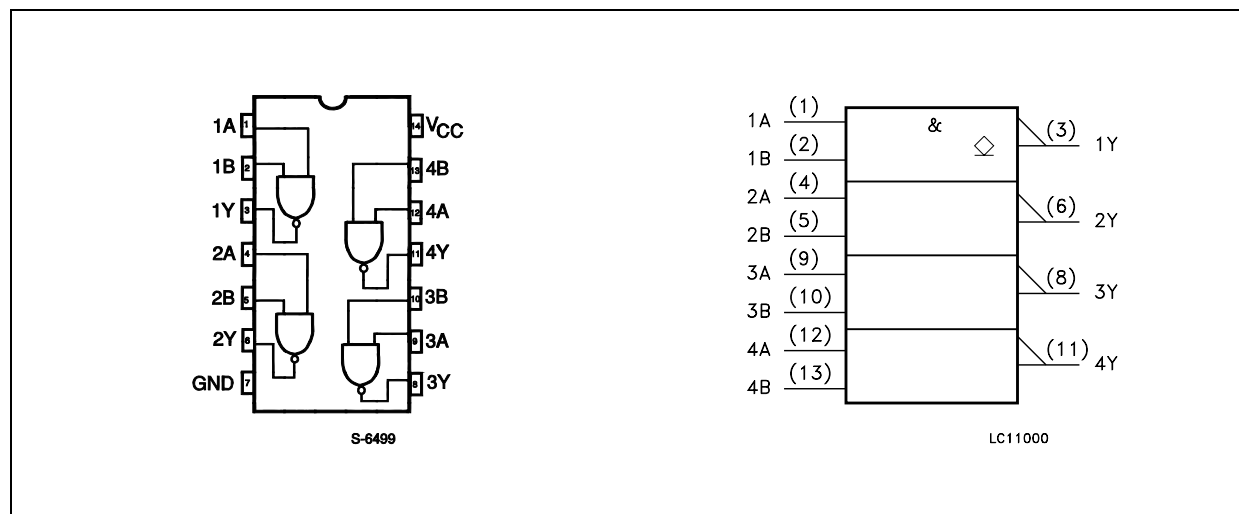
can also be used as a led driver and in any other application requiring a current sink.

Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage.

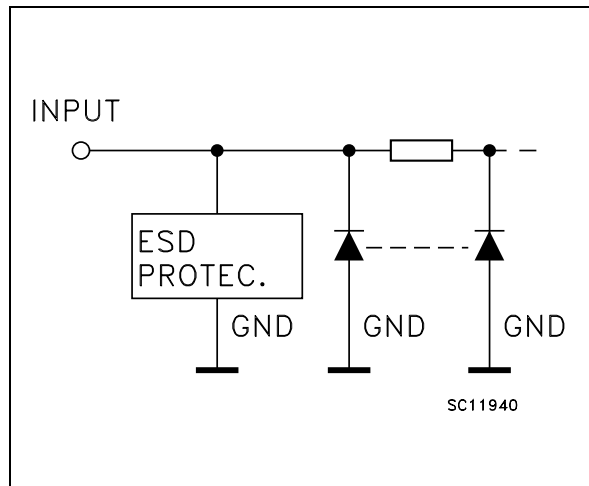
This device can be used to interface 5V to 3V system. It combines high speed performance with the true CMOS low power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data Inputs
2, 5, 10, 13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V _{CC}	Positive Supply Voltage

TRUTH TABLE

A	B	Y
L	L	Z
L	H	Z
H	L	Z
H	H	L

Z: High Impedance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7.0	V
V _I	DC Input Voltage	-0.5 to +7.0	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	- 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Current	± 25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 50	mA
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage (note 1)	2 to 3.6	V
V _I	Input Voltage	0 to 5.5	V
V _O	Output Voltage	0 to V _{CC}	V
T _{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 2) (V _{CC} = 3.3V)	0 to 100	ns/V

1) Truth Table guaranteed: 1.2V to 3.6V

2) V_{IN} from 0.8V to 2.0V

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		3.0		2.0			2.0		2.0		
		3.6		2.4			2.4		2.4		
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		3.0				0.8		0.8		0.8	
		3.6				0.8		0.8		0.8	
V _{OL}	Low Level Output Voltage	2.0	I _O =50 μA		0.0	0.1		0.1		0.1	V
		3.0	I _O =50 μA		0.0	0.1		0.1		0.1	
		3.0	I _O =4 mA			0.36		0.44		0.55	
I _I	Input Leakage Current	3.6	V _I = 5V or GND			± 0.1		± 1		± 1	μA
I _{OZ}	High Impedance Output Leakage Current	3.6	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND			±0.25		± 2.5		± 5.0	μA
I _{CC}	Quiescent Supply Current	3.6	V _I = V _{CC} or GND			2		20		20	μA

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	3.3	C _L = 50 pF		0.3	0.5					V
V _{OLV}				-0.5	-0.3						
V _{IHD}	Dynamic High Voltage Input (note 1, 3)	3.3		2							
V _{ILD}	Dynamic Low Voltage Input (note 1, 3)	3.3				0.8					

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3\text{ns}$)

Symbol	Parameter	Test Condition		Value						Unit	
		V_{CC} (V)	C_L (pF)	$T_A = 25^\circ\text{C}$			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t_{PZL}	Propagation Delay Time	2.7	15		5.4	7.7		9.0		9.5	ns
		2.7	50		6.0	8.7		10.0		11.0	
		3.3 ^(*)	15		4.8	7.0		8.1		8.5	
		3.3 ^(*)	50		5.3	7.6		8.8		9.5	
t_{PLZ}	Propagation Delay Time	2.7	50		10.5	14.7	1.0	15.0	1.0	17.0	ns
		3.3 ^(*)	50		9.6	13.5	1.0	14.0	1.0	15.0	
t_{OSLH} t_{OSHL}	Output To Output Skew Time (note 1, 2)	2.7	50		0.5	1.0		1.5		1.5	ns
		3.3 ^(*)	50		0.5	1.0		1.5		1.5	

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW

2) Parameter guaranteed by design

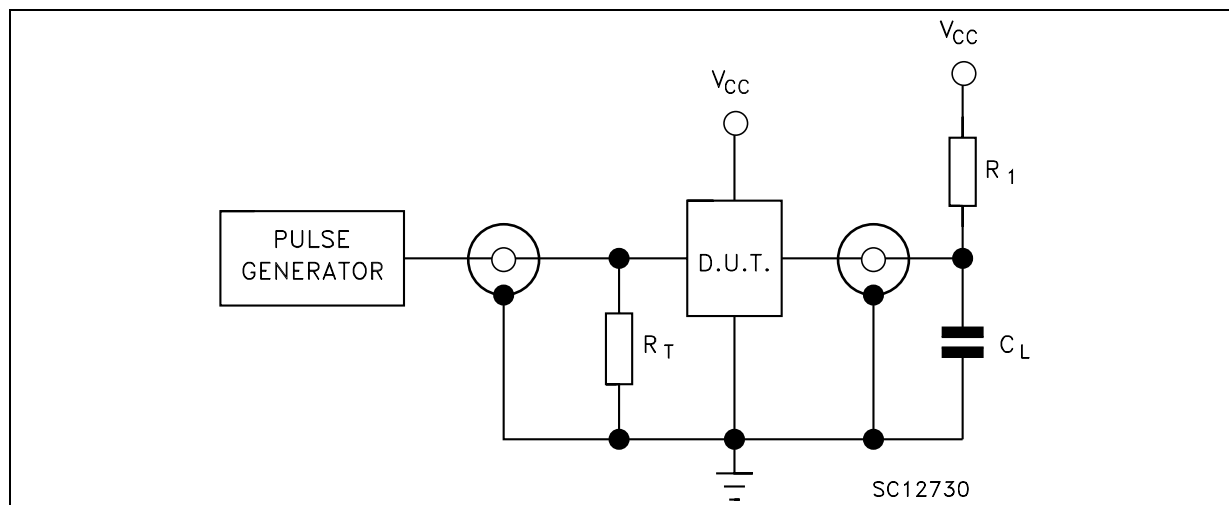
(*) Voltage range is $3.3\text{V} \pm 0.3\text{V}$

CAPACITIVE CHARACTERISTICS

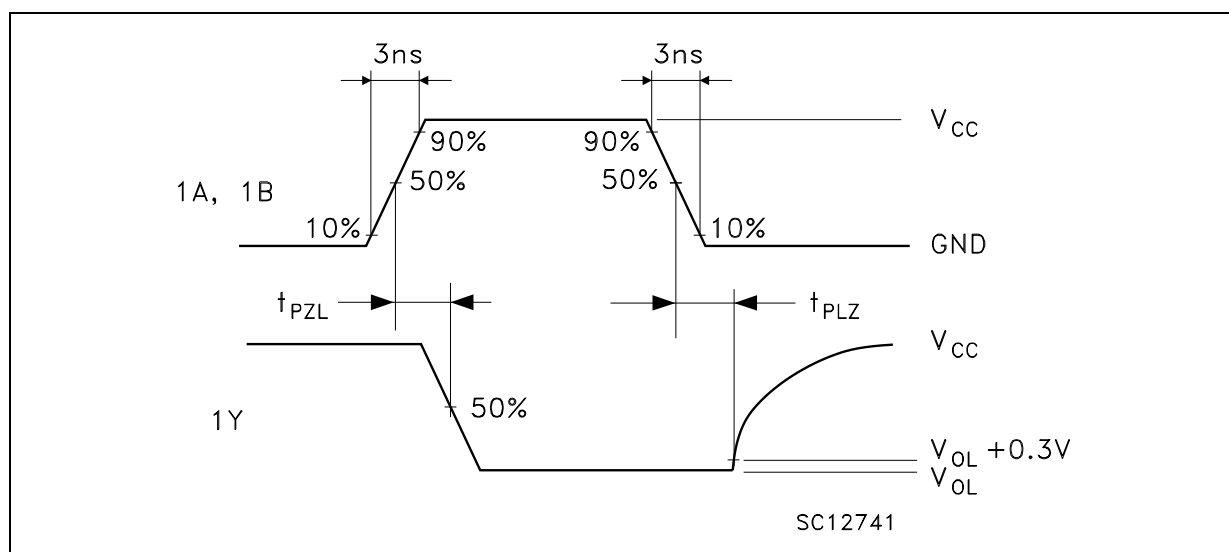
Symbol	Parameter	Test Condition		Value						Unit	
		V_{CC} (V)		$T_A = 25^\circ\text{C}$			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C_{IN}	Input Capacitance	3.3			5.4	10		10		10	pF
C_{OUT}	Output Capacitance	3.3			7.3						pF
C_{PD}	Power Dissipation Capacitance (note 1)	3.3			2.6						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/6$ (per gate)

TEST CIRCUIT

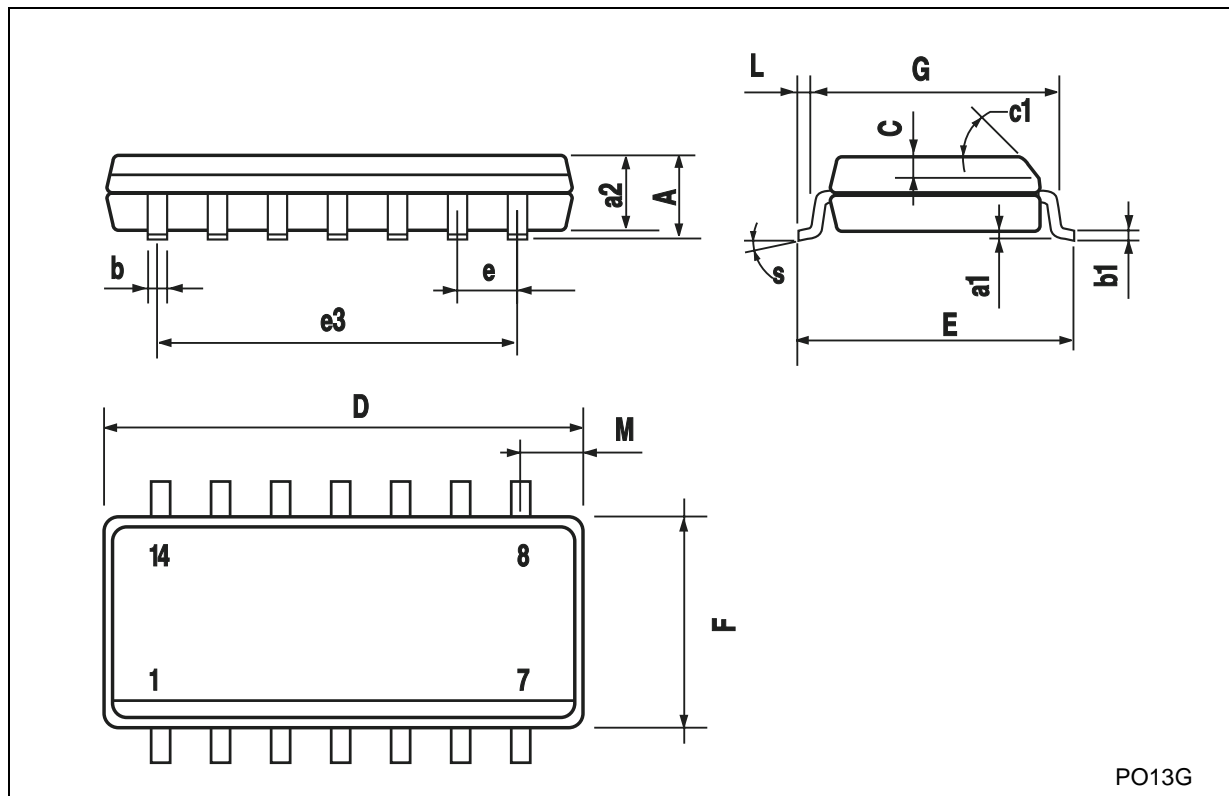


$C_L = 15/50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_L = R_1 = 1\text{K}\Omega$ or equivalent
 $R_T = Z_{\text{OUT}}$ of pulse generator (typically 50Ω)

WAVEFORM : PROPAGATION DELAYS ($f=1\text{MHz}$; 50% duty cycle)

SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



PO13G

TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>