Philips Components

Data sheet	
status	Preliminary specification
date of issue	September 1990

74HC/HCT595

8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

FEATURES

- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- 100 MHz (typ) shift out frequency
- Output capability:
  - parallel outputs; bus driver
  - serial output; standard
- I_{CC} category: MSI

APPLICATIONS

- Serial-to-parallel data conversion
- Remote control holding register

DESCRIPTION

The 74HC/HCT595 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The "595" is an 8-stage serial shift register with a storage register and 3-state outputs. The shift register and storage register have separate clocks.

Data is shifted on the positive-going transitions of the SH_{CP} input. The data in each register is transferred to the storage register on a positive-going transition of the ST_{CP} input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register.

The shift register has a serial input (D_S) and a serial standard output (Q_7') for cascading. It is also provided with asynchronous reset (active LOW) for all 8 shift register stages. The storage register has 8 parallel 3-state bus driver outputs. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is LOW.

PIN CONFIGURATION

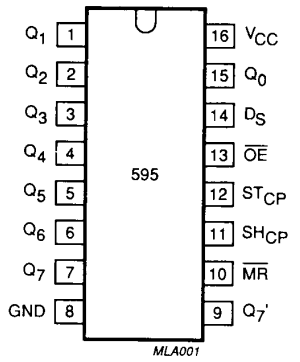

Fig.1 Pin configuration.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT595P	16	DIL	plastic	SOT38Z
74HC/HCT595T	16	SO16	plastic	SOT109A

tab 5

PHILIPS

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74HC/HCT595

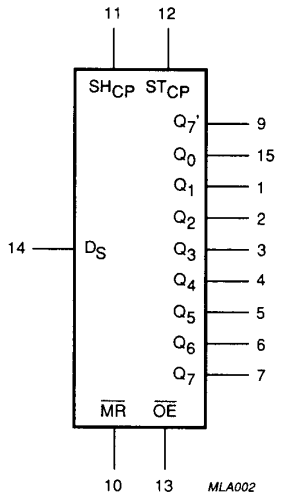

Fig.2 Logic symbol.

PINNING

SYMBOL	PIN	DESCRIPTION
Q_0 - Q_7	15, 1 - 7	parallel data outputs
GND	8	ground (0 V)
Q_7'	9	serial data output
$\overline{MR}$	10	master reset (active LOW)
SH_{CP}	11	shift register clock input
ST_{CP}	12	storage register clock input
$\overline{OE}$	13	output enable (active LOW)
D_S	14	serial data input
V_{CC}	16	positive supply voltage

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay SH_{CP} to Q_7' ST_{CP} to Q_n $\overline{MR}$ to Q_7'	C_L = 15 pF V_{CC} = 5 V	 16 17 14	 21 20 19	 ns ns ns
f_{max}	maximum clock frequency SH_{CP}, ST_{CP}		100	57	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	115	130	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz C_L = output load capacitance in pF
   f_o = output frequency in MHz V_{CC} = supply voltage in V
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} - 1.5 V.

8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

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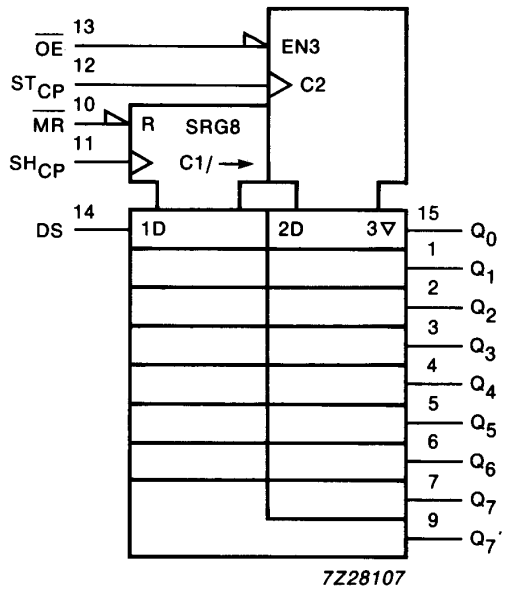


Fig.3 IEC logic symbol.

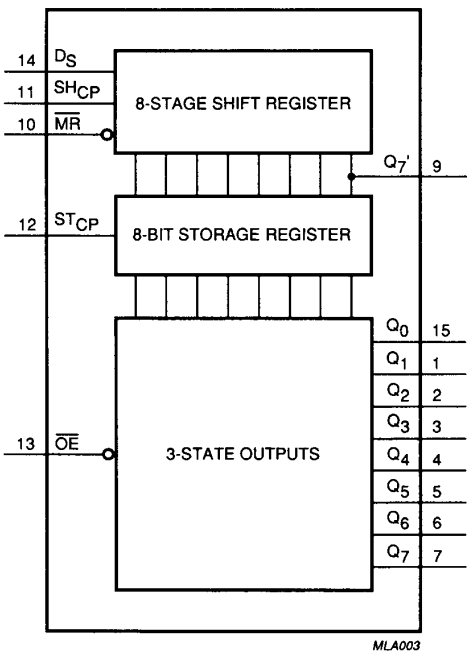


Fig.4 Functional diagram.

8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

74HC/HCT595

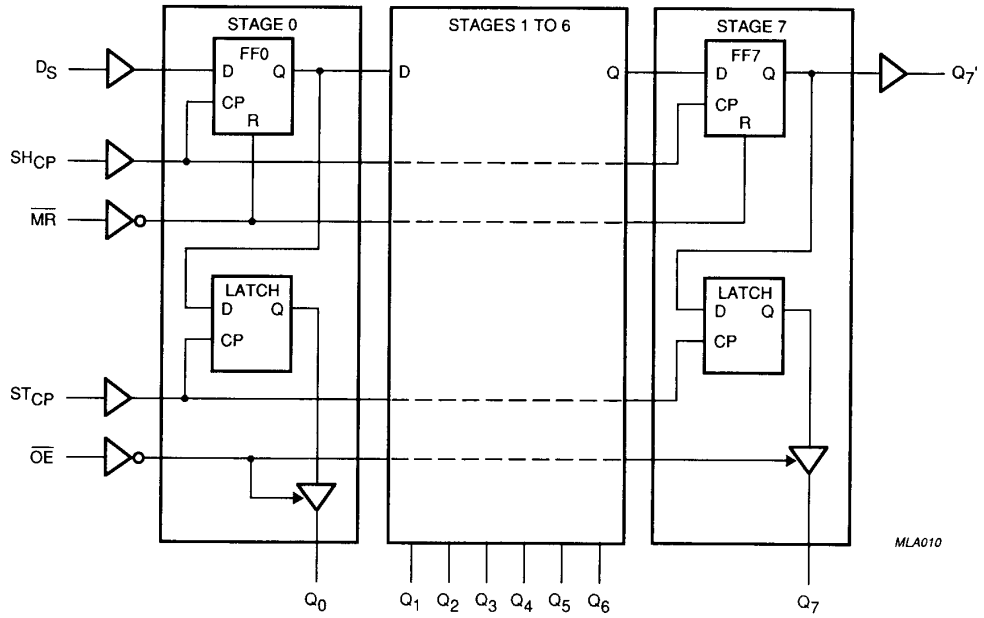


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS					OUTPUTS		FUNCTION
SH_{CP}	ST_{CP}	$\overline{OE}$	$\overline{MR}$	D_S	Q_7'	Q_n	
X	X	L	↓	X	L	NC	a LOW level on $\overline{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear. Parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q_6'	NC	logic high level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q_6') appears on the serial output (Q_7')
X	↑	L	H	X	NC	Q_n'	contents of shift register stages (internal Q_n') are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q_6'	Q_n'	contents of shift register shifted through. Previous contents of the shift register is transferred to the storage register and the parallel output stages

H = HIGH voltage level
L = LOW voltage level
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
Z = high-impedance OFF-state
NC = no change
X = don't care.

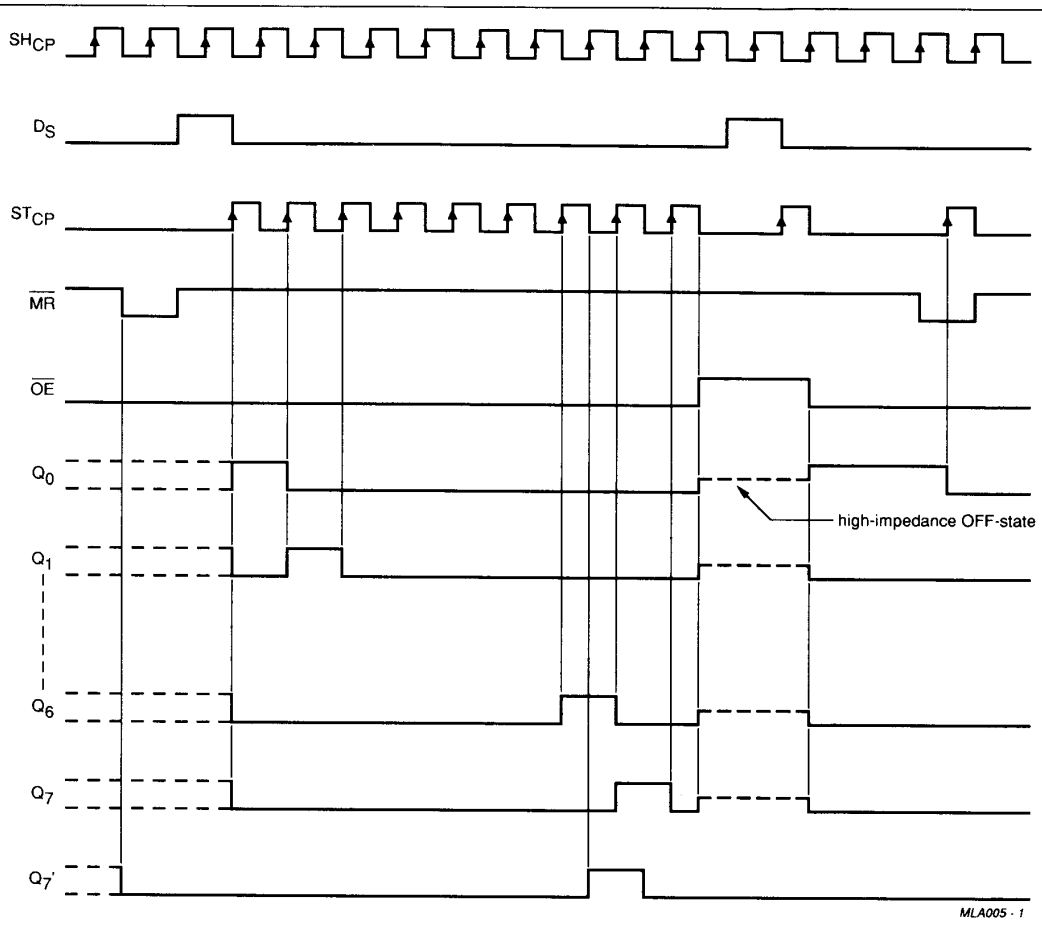


Fig.6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: parallel outputs, bus driver; serial output, standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb}(°C)							UNIT	TESTCONDITION	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to+85		−40 to+125				
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/ t_{PLH}	propagation delay SH_{CP} to Q_7'		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig.7
t_{PHL}/ t_{PLH}	propagation delay ST_{CP} to Q_n		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.8
t_{PHL}	propagation delay $\overline{MR}$ to Q_7'		47 17 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.10
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.11
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.11
t_W	shift clock pulse width HIGH or LOW	75 15 13	17 6 5		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig.7
t_W	storage clock pulse width HIGH or LOW	75 15 13	11 4 3		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig.8
t_W	master reset pulse width LOW	75 15 13	17 6 5		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig.10
t_{su}	set-up time D_S to SH_{CP}	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.9
t_{su}	set-up time SH_{CP} to ST_{CP}	75 15 13	22 8 7		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig.8

SYMBOL	PARAMETER	T_{amb}(°C)								UNIT	TESTCONDITION	
		74HC									V_{CC} V	WAVEFORMS
		+25			−40 to+85		−40 to+125					
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.				
t_h	hold time D_S to SH_{CP}	3	−6		3		3			ns	2.0	Fig.9
		3	−2		3		3				4.5	
		3	−2		3		3				6.0	
t_{rem}	removal time $\overline{MR}$ to SH_{CP}	50	−19		65		75			ns	2.0	Fig.10
		10	−7		13		15				4.5	
		9	−6		11		13				6.0	
f_{max}	maximum clock pulse frequency SH_{CP} or ST_{CP}	6.0	30		4.8		4.0			MHz	2.0	Figs 7 and 8
		30	91		24		20				4.5	
		35	108		28		24				6.0	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: parallel outputs, bus driver; serial output, standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D_S	0.25
$\overline{MR}$	1.50
SH_{CP}	1.50
ST_{CP}	1.50
$\overline{OE}$	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb}(°C) 74HCT +25 MIN.	+25 TYP.	+25 MAX.	−40 to+85 MIN.	−40 to+85 MAX.	−40 to+125 MIN.	−40 to+125 MAX.	UNIT	TESTCONDITION V_{CC} V	TESTCONDITION WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q_7'		25	42		53		63	ns	4.5	Fig.7
t_{PHL}/t_{PLH}	propagation delay ST_{CP} to Q_n		24	40		50		60	ns	4.5	Fig.8
t_{PHL}	propagation delay $\overline{MR}$ to Q_7'		23	40		50		60	ns	4.5	Fig.10
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n		21	35		44		53	ns	4.5	Fig.11
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n		18	30		38		45	ns	4.5	Fig.11
t_W	shift clock pulse width HIGH or LOW	16	6		20		24		ns	4.5	Fig.7
t_W	storage clock pulse width HIGH or LOW	16	5		20		24		ns	4.5	Fig.8
t_W	master reset pulse width LOW	20	8		25		30		ns	4.5	Fig.10
t_{su}	set-up time D_S to SH_{CP}	16	5		20		24		ns	4.5	Fig.9
t_{su}	set-up time SH_{CP} to ST_{CP}	16	8		20		24		ns	4.5	Fig.8
t_h	hold time D_S to SH_{CP}	3	−2		3		3		ns	4.5	Fig.9
t_{rem}	removal time $\overline{MR}$ to SH_{CP}	10	−7		13		15		ns	4.5	Fig.10
f_{max}	maximum clock pulse frequency SH_{CP} or ST_{CP}	30	52		24		20		MHz	4.5	Figs 7 and 8

AC WAVEFORMS

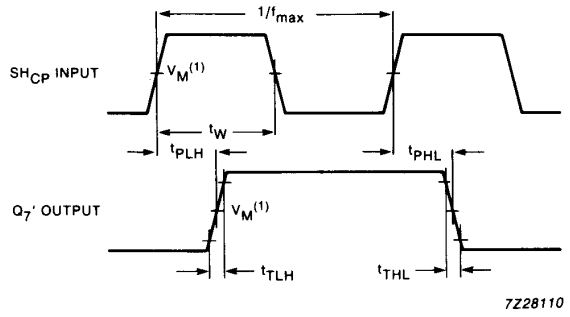


Fig.7 Waveforms showing the clock (SH_{CP}) to output (Q_7') propagation delays, the shift clock pulse width and maximum shift clock frequency.

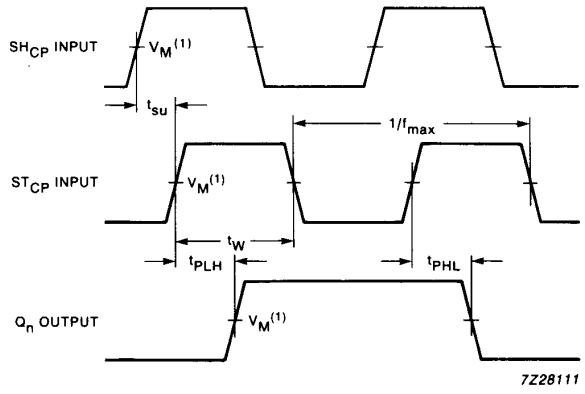


Fig.8 Waveforms showing the storage clock (ST_{CP}) to output (Q_n) propagation delays, the storage clock pulse width and the shift clock to storage clock set-up time.

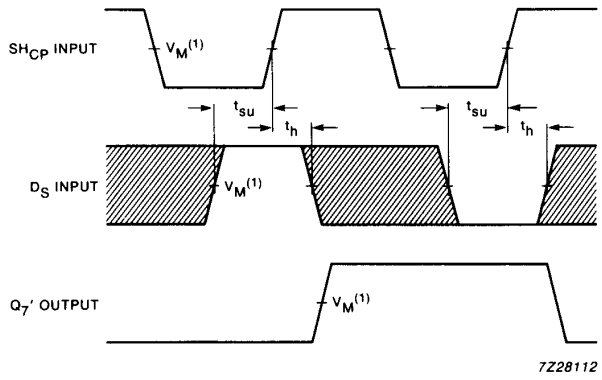


Fig.9 Waveforms showing the data set-up and hold times for the D_S input.

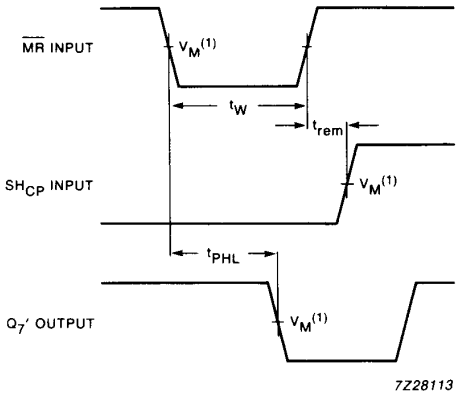


Fig.10 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Q_7') propagation delay and the master reset to shift clock (SH_{CP}) removal time.

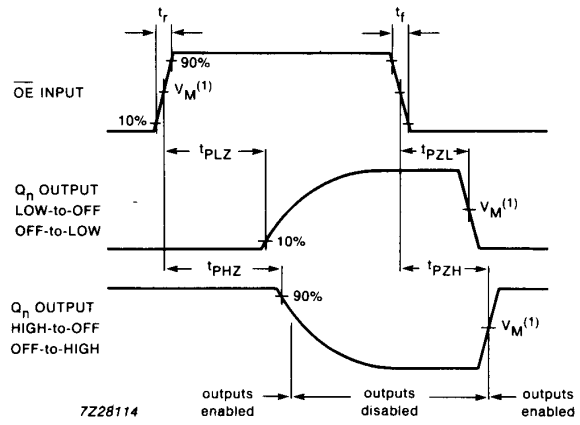
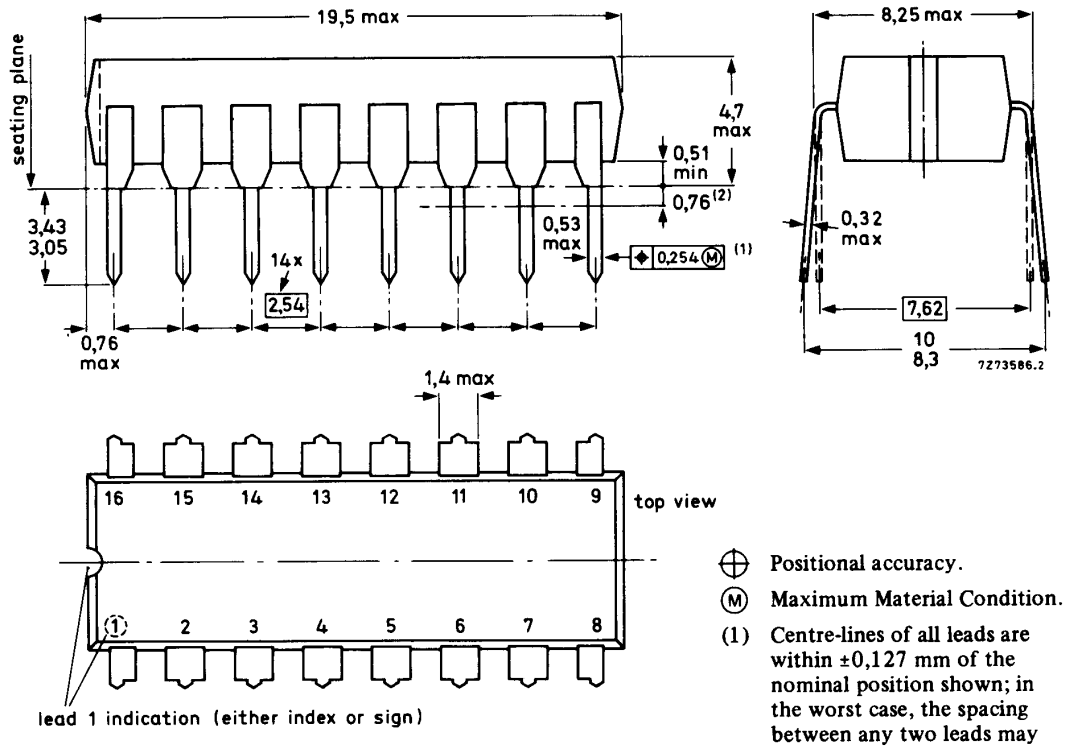


Fig.11 Waveforms showing the 3-state enable and disable times for input $\overline{OE}$.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}
HCT: V_M = 1.3 V; V_I = GND to 3 V.

PACKAGE OUTLINES



⊕ Positional accuracy.

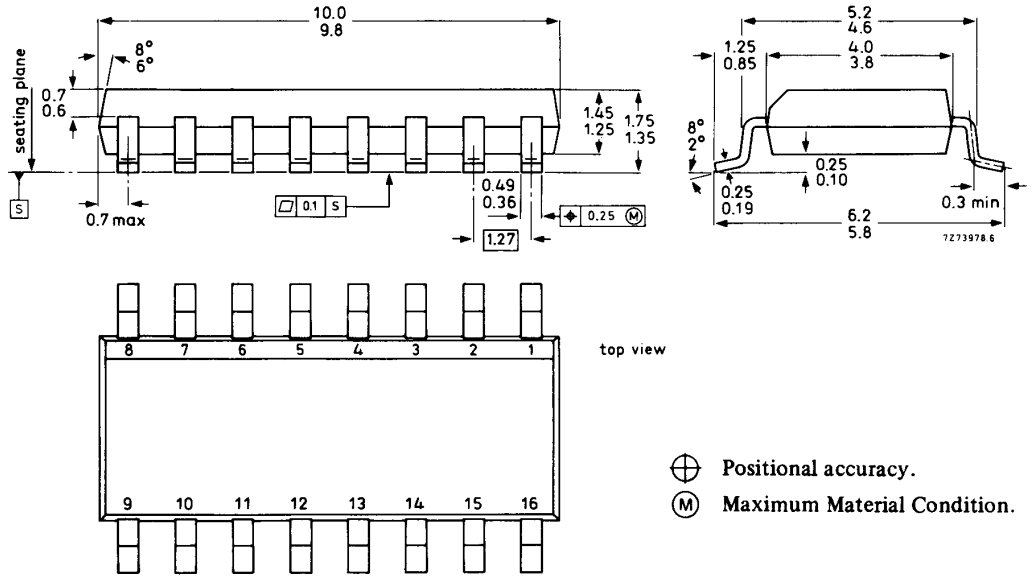
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

Fig.12 16-lead dual in-line; plastic (SOT38Z).



Dimensions in mm

Fig.13 16-lead mini-pack; plastic (SO16; SOT109A).

SOLDERING PLASTIC MINI-PACKS

By hand-held soldering iron or pulse-heated solder tool

Fix the component by first soldering two, diagonally opposite, end leads. Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

Pre-heating is necessary to dry the paste and evaporate the binding agent.

Pre-heating duration: 45 minutes at 45 °C.

Repairing soldered joints

The same precautions and limits apply as in (1) above.

SOLDERING PLASTIC DUAL IN-LINE PACKAGES

By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 and 400 °C, for not more than 5 seconds.

By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

The same precautions and limits apply as in (1) above.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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