HARRIS Semiconductor

RFL1N18, RFL1N20

1A, 180V and 200V, 3.65 Ohm, N-Channel Power MOSFETs

January 1998

Features

- **1A, 180V and 200V**
- **$r_{DS(ON)}$ = 3.65Ω**
- **SOA is Power Dissipation Limited**
- **Nanosecond Switching Speeds**
- **Linear Transfer Characteristics**
- **High Input Impedance**
- **Majority Carrier Device**
- **Related Literature**
  - **TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”**

Description

These are N-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

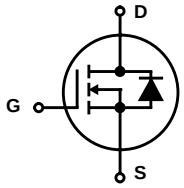
Formerly developmental type TA09289.

Ordering Information

PART NUMBER	PACKAGE	BRAND
RFL1N18	TO-205AF	RFL1N18
RFL1N20	TO-205AF	RFL1N20

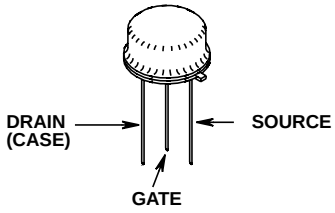
NOTE: When ordering, use the entire part number.

Symbol



Packaging

JEDEC TO-205AF



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **1442.2**

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFL1N18	RFL1N20	UNITS
Drain to Source Breakdown Voltage (Note 1)	V_{DS}	180	200	V
Drain to Gate Voltage (R_{GS} = 1MΩ) (Note 1)	V_{DGR}	180	200	V
Continuous Drain Current	I_D	1	1	A
Pulsed Drain Current	I_{DM}	5	5	A
Gate to Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation	P_D	8.33	8.33	W
Linear Derating Factor		0.0667	0.0667	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	-55 to 150	^oC
Maximum Temperature for Soldering				
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V					
RFL1N18				180	-	-	V
RFL1N20				200	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA, (Figure 8)		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x Rated BV_{DSS}	$T_C = 25^oC$	-	-	1	μA
			$T_C = 125^oC$	-	-	25	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V		-	-	±100	nA
Drain to Source On-Voltage (Note 2)	$V_{DS(ON)}$	I_D = 1A, V_{GS} = 10V		-	-	3.65	V
		I_D = 2A, V_{GS} = 10V		-	-	8.3	V
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 1A, V_{GS} = 10V, (Figures 6, 7)		-	-	3.65	Ω
Forward Transconductance (Note 2)	g_{fs}	I_D = 1A, V_{DS} = 10V, (Figure 10)		400	-	-	S
Turn-On Delay Time	$t_{d(ON)}$	$I_D \approx$ 1A, V_{DD} = 100V R_{GS} = 50Ω, V_{GS} = 10V, (Figures 11, 12, 13)		-	15	25	ns
Rise Time	t_r			-	20	30	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	25	40	ns
Fall Time	t_f			-	30	50	ns
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz, (Figure 9)		-	-	200	pF
Output Capacitance	C_{OSS}			-	-	60	pF
Reverse Transfer Capacitance	C_{RSS}			-	-	25	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	15	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = 1A	-	-	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_{SD} = 2A, dI_{SD}/dt = 50A/μs	-	200	-	ns

NOTE:

2. Pulse test: pulse width ≤ 300μs maximum, duty cycle ≤ 2%.

Typical Performance Curves Unless Otherwise Specified

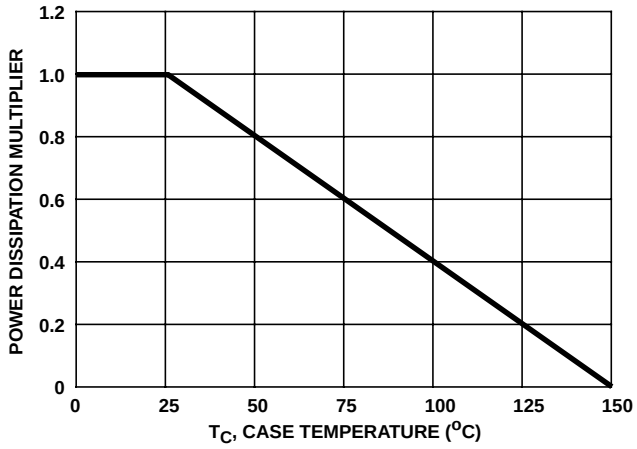


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

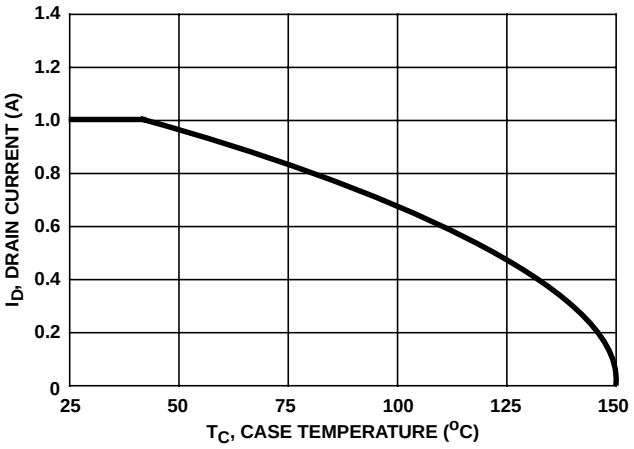


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

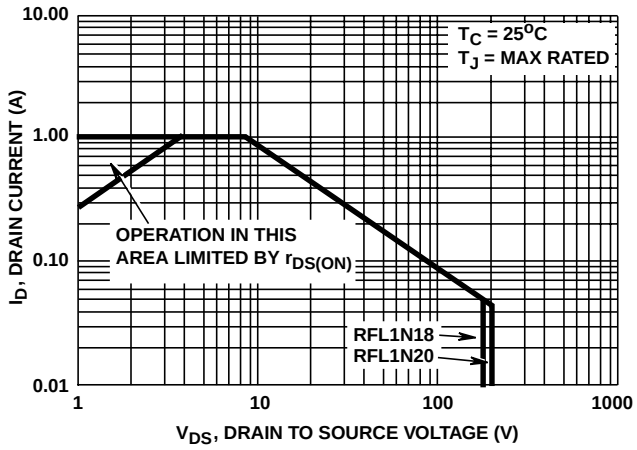


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

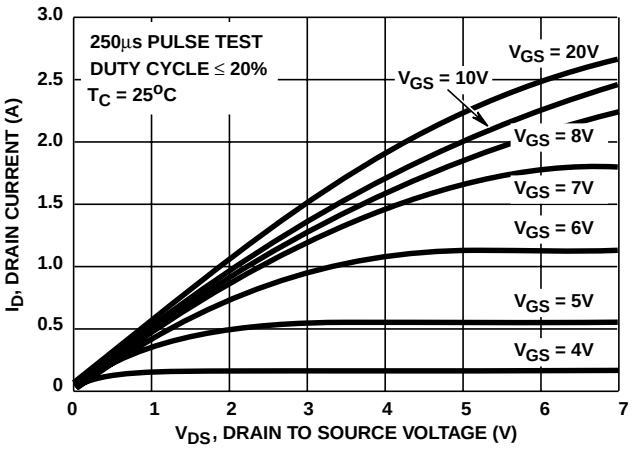


FIGURE 4. SATURATION CHARACTERISTICS

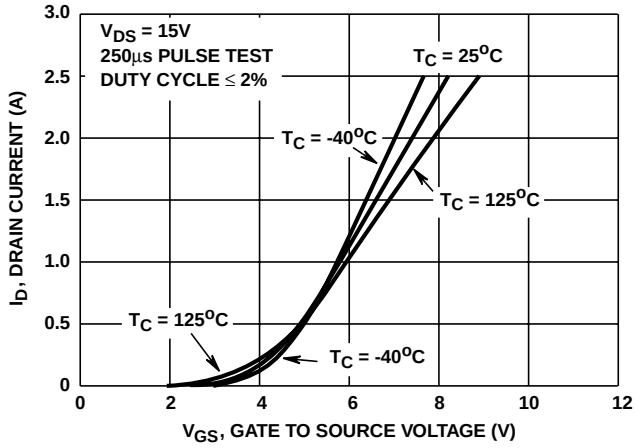


FIGURE 5. TRANSFER CHARACTERSTICS

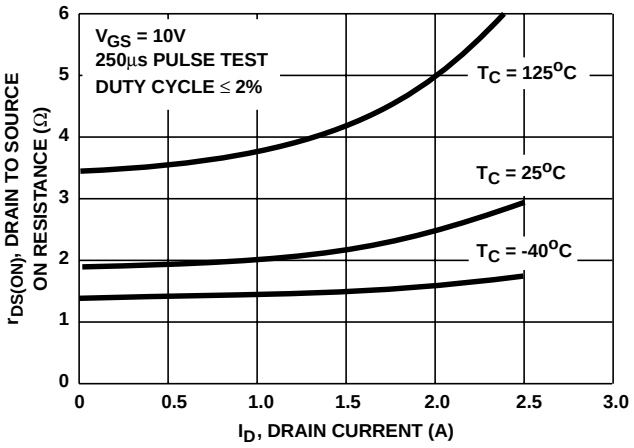


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

Typical Performance Curves Unless Otherwise Specified (Continued)

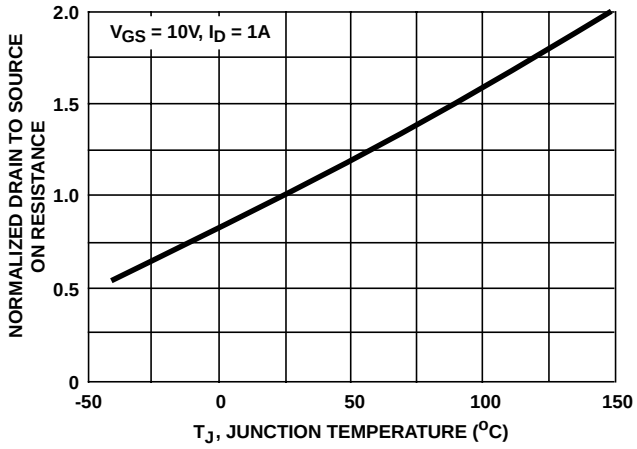


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

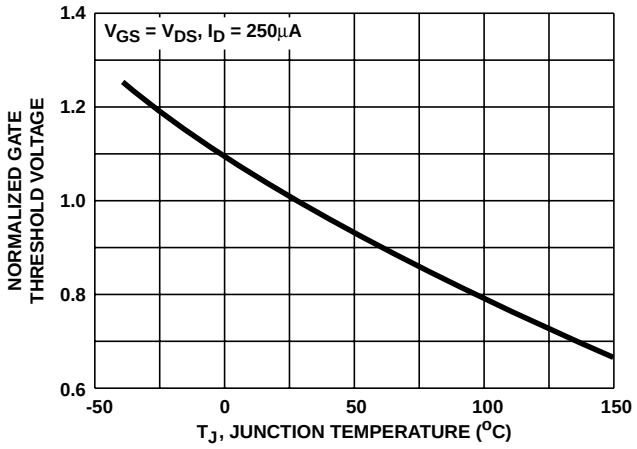


FIGURE 8. NORMALIZED GATE THRESHOLD vs JUNCTION TEMPERATURE

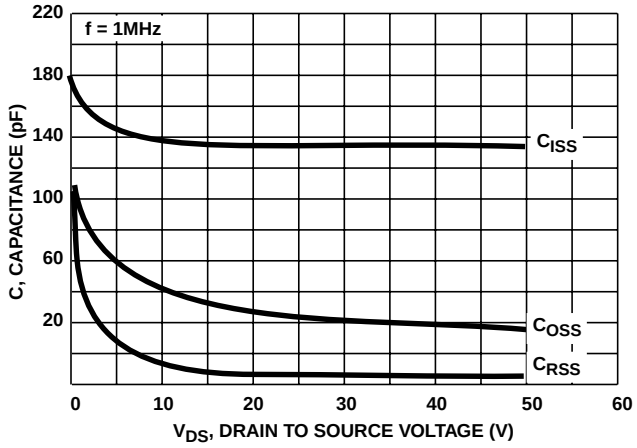


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

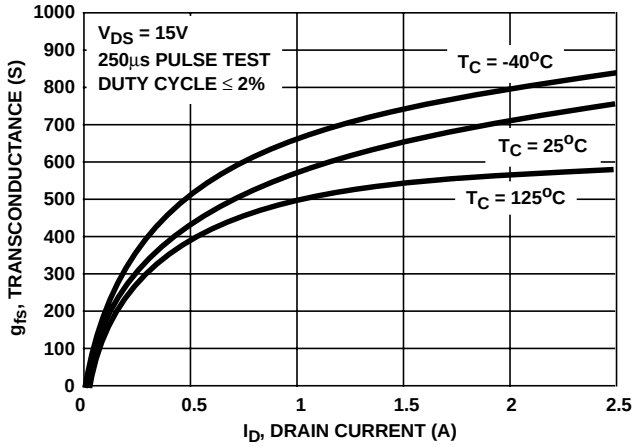
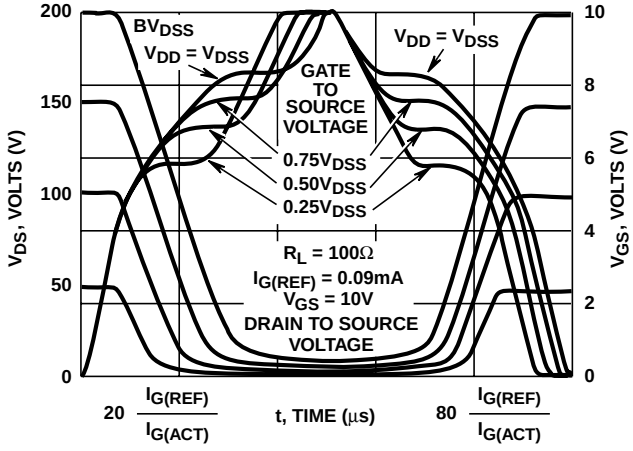


FIGURE 10. TRANSCONDUCTANCE vs DRAIN CURRENT



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuit and Waveforms

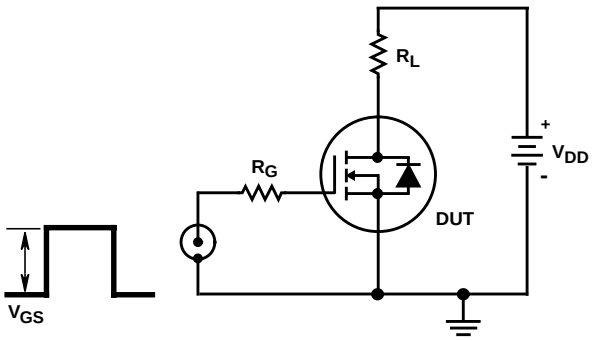


FIGURE 12. SWITCHING TIME TEST CIRCUIT

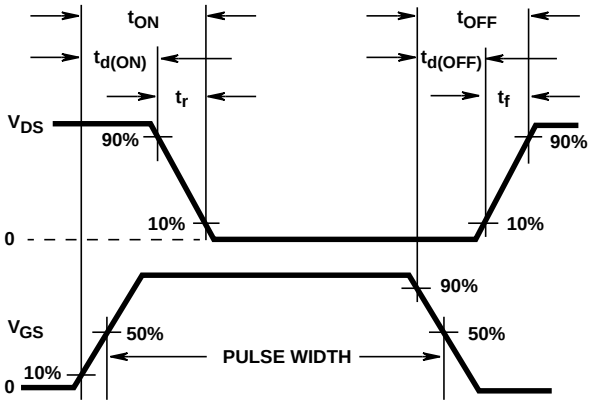


FIGURE 13. RESISTIVE SWITCHING WAVEFORMS