Data Sheet October 1999 File Number 1560.3

2A, 60V, 0.950 Ohm, Logic Level, N-Channel Power MOSFET

The RFL2N06L N-channel enhancement mode silicon gate power field effect transistor is designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA9520.

Ordering Information

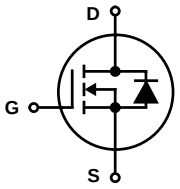
PART NUMBER	PACKAGE	BRAND
RFL2N06L	TO-205AF	RFL2N06L

NOTE: When ordering, use the entire part number.

Features

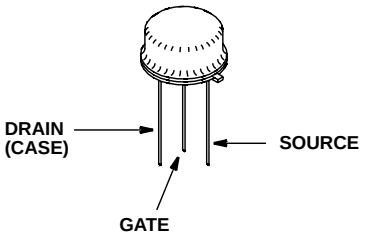
- 2A, 50V and 60V
- $r_{DS(ON)} = 0.950\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Symbol



Packaging

JEDEC TO-205AF



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFL2N06L	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	50	V
Drain to Gate Voltage (R_{GS} = 20KΩ) (Note 1)	V_{DGR}	60	V
Continuous Drain Current	I_D	2	A
Pulsed Drain Current (Note 3)	I_{DM}	10	A
Gate to Source Voltage	V_{GS}	±10	V
Maximum Power Dissipation	P_D	8.33	W
Above $T_C = 25^oC$, Derate Linearly		0.0667	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V	60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA, (Figure 8)	1	-	2	V
Zero Gate Voltage Drain Current	IDSS	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_C = 125^oC$	-	-	25	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0V	-	-	±100	nA
Drain to Source On Voltage (Note 2)	$V_{DS(ON)}$	I_D = 2A, V_{GS} = 5V	-	-	1.9	V
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D =2A, V_{GS} = 5V, (Figures 6, 7)		-	0.950	Ω
Turn-On Delay Time	$t_{d(ON)}$	I_D = 2A, V_{DD} = 30V, R_G = 6.25Ω, R_L = 30Ω V_{GS} = 5V, (Figures 10, 11, 12)	-	10	20	ns
Rise Time	t_r		-	65	130	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	20	40	ns
Fall Time	t_f		-	30	60	ns
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz, (Figure 9)	-	-	225	pF
Output Capacitance	C_{OSS}		-	-	100	pF
Reverse Transfer Capacitance	C_{RSS}		-	-	40	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	15	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = 2A	-	-	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_{SD} = 2A, dI_{SD}/dt = 100A/μs	-	150	-	ns

NOTES:

2. Pulse test: pulse width ≤ 300μs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

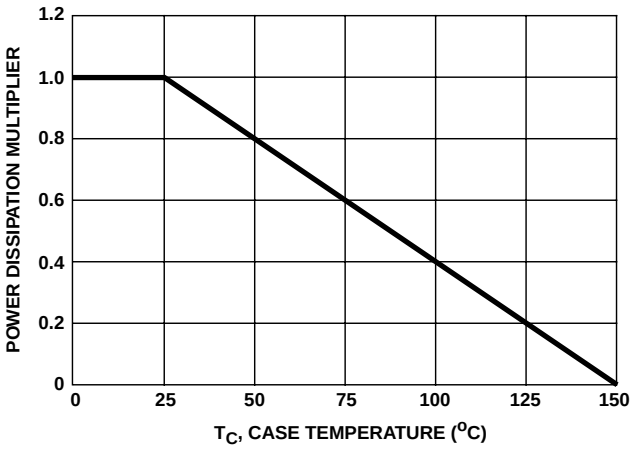


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

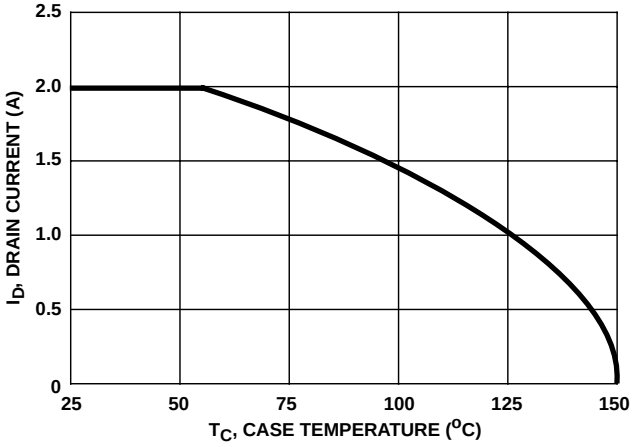


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

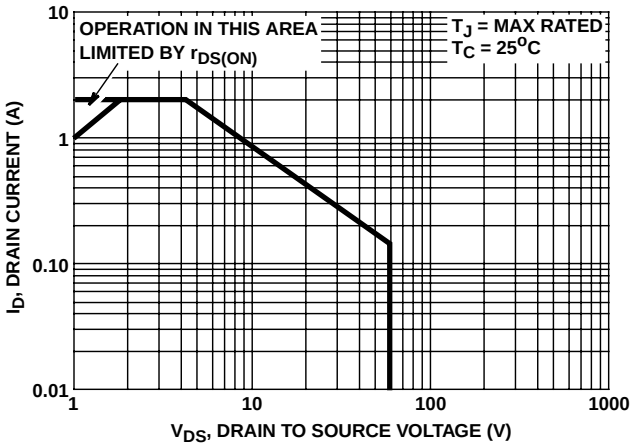


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

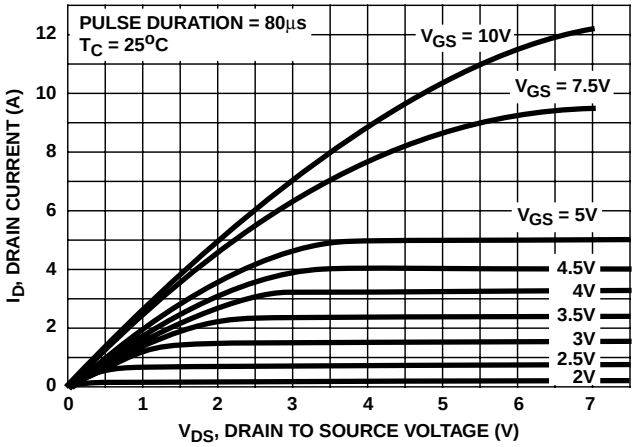


FIGURE 4. SATURATION CHARACTERISTICS

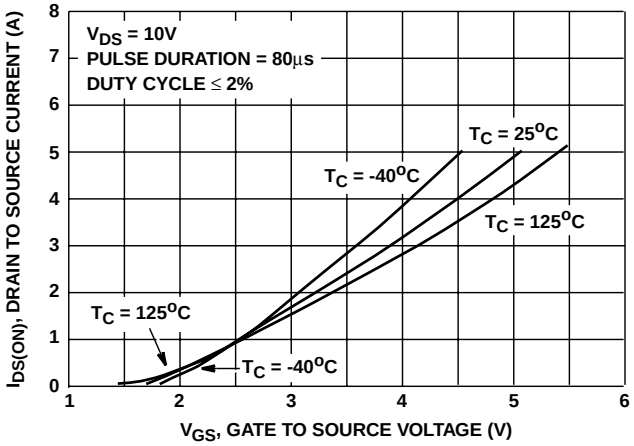


FIGURE 5. TRANSFER CHARACTERISTICS

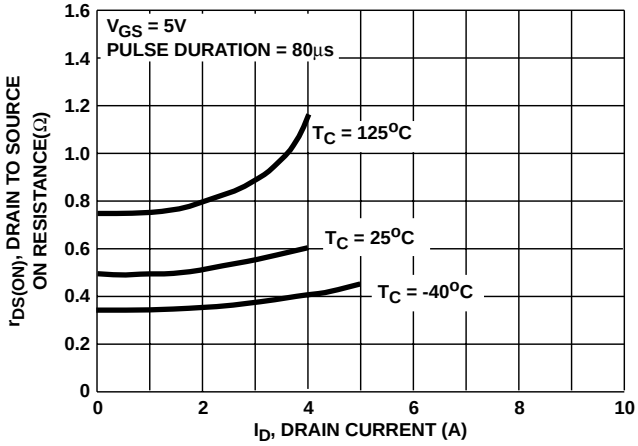


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

Typical Performance Curves Unless Otherwise Specified **(Continued)**

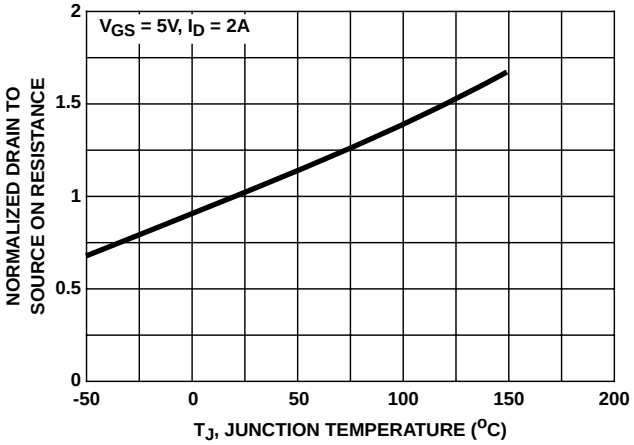


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

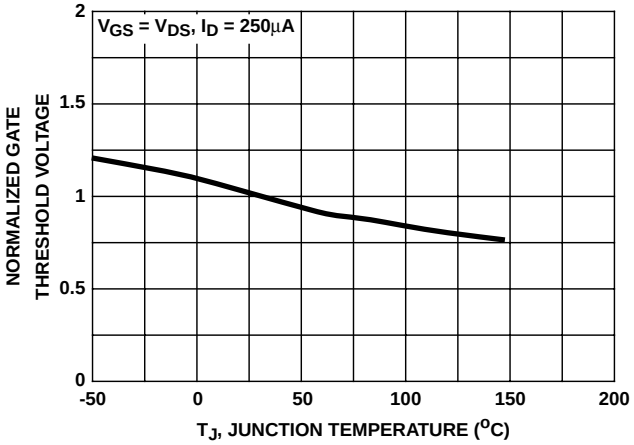


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

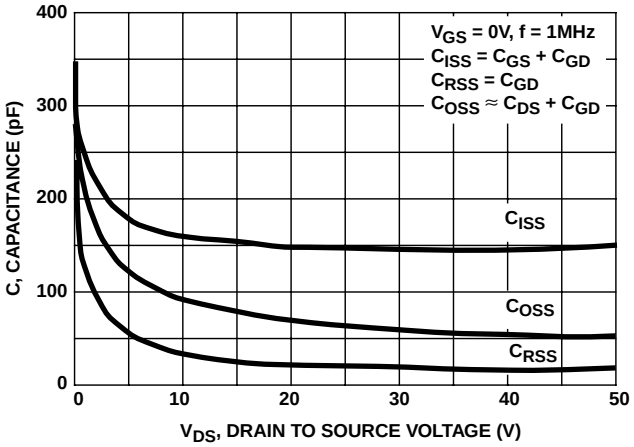
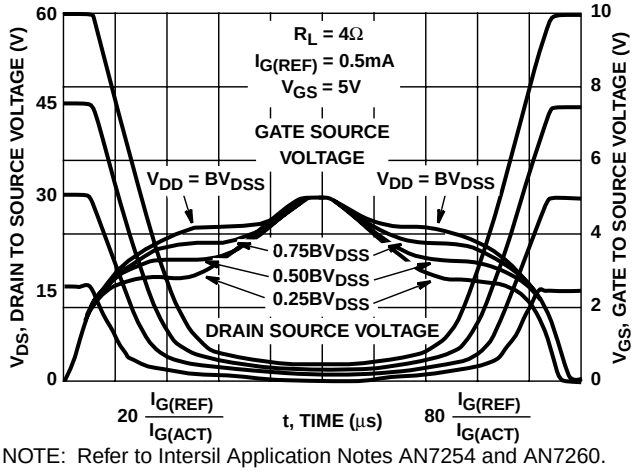


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

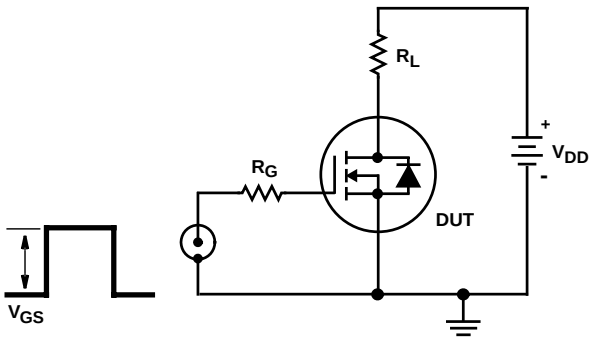


FIGURE 11. SWITCHING TIME TEST CIRCUIT

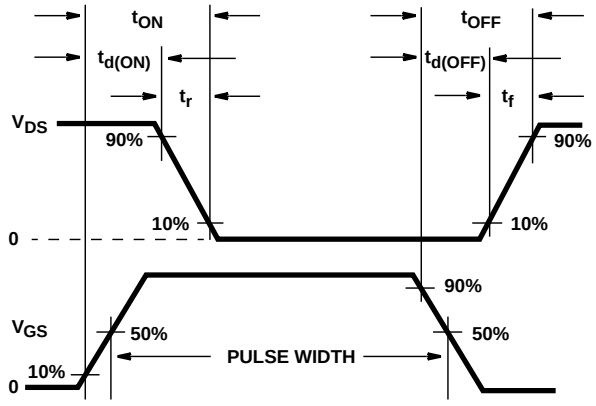


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

For information regarding Intersil Corporation and its products, see web site **www.intersil.com**

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029