18A, 200V, 0.180 Ohm, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17422.

Ordering Information

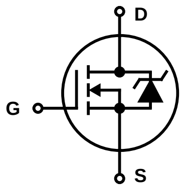
PART NUMBER	PACKAGE	BRAND
IRF240	TO-204AE	IRF240

NOTE: When ordering, include the entire part number.

Features

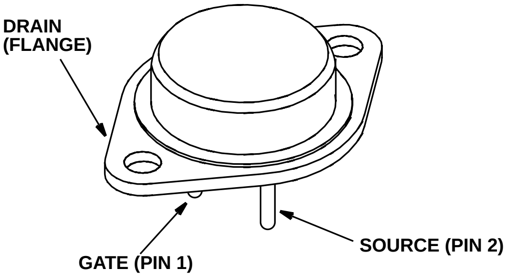
- 18A, 200V
- $r_{DS(ON)} = 0.180\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
  - TB334, “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol



Packaging

JEDEC TO-204AE
TOP VIEW



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

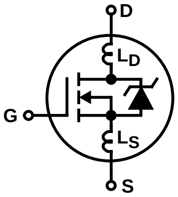
		IRF240	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	200	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	200	V
Continuous Drain Current	I_D	18	A
$T_C = 100^oC$	I_D	11	A
Pulsed Drain Current (Note 3)	I_{DM}	72	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	125	W
Linear Derating Factor		1.0	$W/^oC$
Single Pulse Avalanche Energy Rating (Note 4)	E_{AS}	580	mJ
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

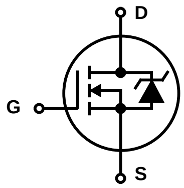
NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V$, $I_D = 250\mu A$ (Figure 10)	200	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	2.0	-	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, $V_{GS} = 0V$	-	-	25	µA
		V_{DS} = 0.8 x Rated BV_{DSS}, $V_{GS} = 0V$, $T_J = 125^oC$	-	-	250	µA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, $V_{GS} = 10V$	18	-	-	A
Gate to Source Leakage	I_{GSS}	$V_{GS} = \pm 20V$	-	-	±100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	$V_{GS} = 10V$, $I_D = 10A$ (Figures 8, 9)	-	0.14	0.180	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} = 10V$, $I_D = 11V$ (Figure 12)	6.7	9.0	-	S
Turn-On Delay Time	$t_{D(ON)}$	$V_{DD} = 100V$, $I_D \approx 18A$, $R_G = 9.1\Omega$, $R_L = 5.3\Omega$ (Figures 17, 18) MOSFET Switching Times are Essentially Independent of Operating Temperature	-	16	30	ns
Rise Time	t_r		-	27	60	ns
Turn-Off Delay Time	$t_{D(OFF)}$		-	40	80	ns
Fall Time	t_f		-	31	60	ns
Total Gate Charge (Gate to Source + Gate to Drain)	Q_g	$V_{GS} = 10V$, $I_D = 18A$, V_{DS} = 0.8 x Rated BV_{DSS}, $I_{g(REF)} = 1.5mA$ (Figures 14, 19, 20) Gate Charge is Essentially Independent of Operating Temperature	-	43	60	nC
Gate to Source Charge	Q_{gs}		-	8	-	nC
Gate to Drain “Miller” Charge	Q_{gd}		-	27	-	nC
Input Capacitance	C_{ISS}	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1.0MHz (Figure 11)	-	1275	-	pF
Output Capacitance	C_{OSS}		-	500	-	pF
Reverse-Transfer Capacitance	C_{RSS}		-	160	-	pF
Internal Drain Inductance	L_D	Measured between the Contact Screw on Header that is Closer to Source and Gate Pins and Center of Die Modified MOSFET Symbol Showing the Internal Devices Inductances 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the Source Lead, 6mm (0.25in) from Header to Source Bonding Pad	-	12.5	-	nH
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	1.0	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation	-	-	30	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode 	-	-	18	A
Pulse Source to Drain Current (Note 3)	I_{SM}		-	-	72	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^oC$, $I_{SD} = 18A$, $V_{GS} = 0V$ (Figure 13)	-	-	2.0	V
Reverse Recovery Time	t_{rr}	$T_J = 150^oC$, $I_{SD} = 18A$, $dI_{SD}/dt = 100A/\mu s$	-	650	-	ns
Reverse Recovered Charge	Q_{RR}	$T_J = 150^oC$, $I_{SD} = 18A$, $dI_{SD}/dt = 100A/\mu s$	-	4.1	-	μC

NOTES:

2. Pulse Test: Pulse width ≤ 300μs, duty cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. $V_{DD} = 50V$, starting $T_J = 25^oC$, $L = 2.7mH$, $R_G = 25\Omega$, peak $I_{AS} = 9A$. See Figures 15 and 16.

Typical Performance Curves Unless Otherwise Specified

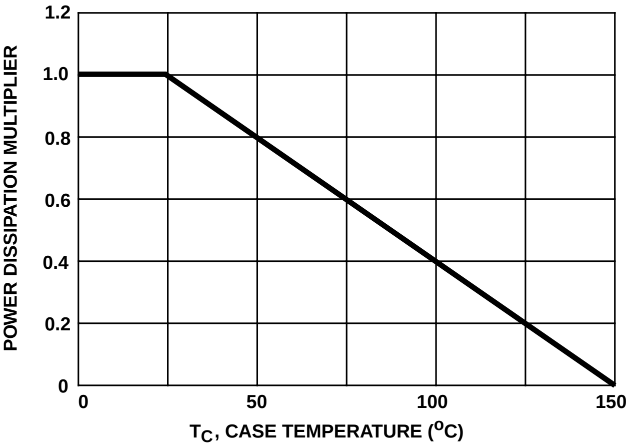


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

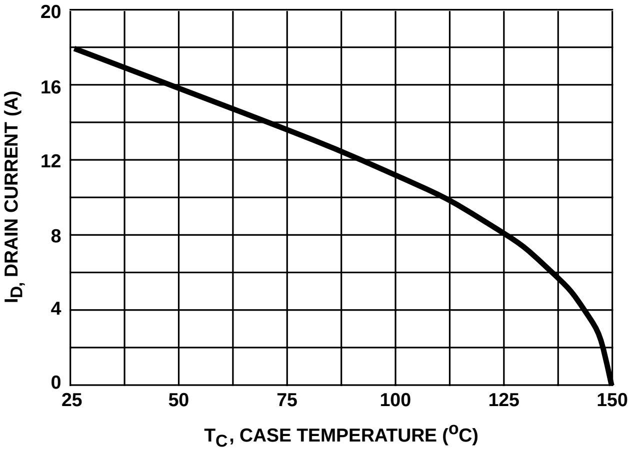
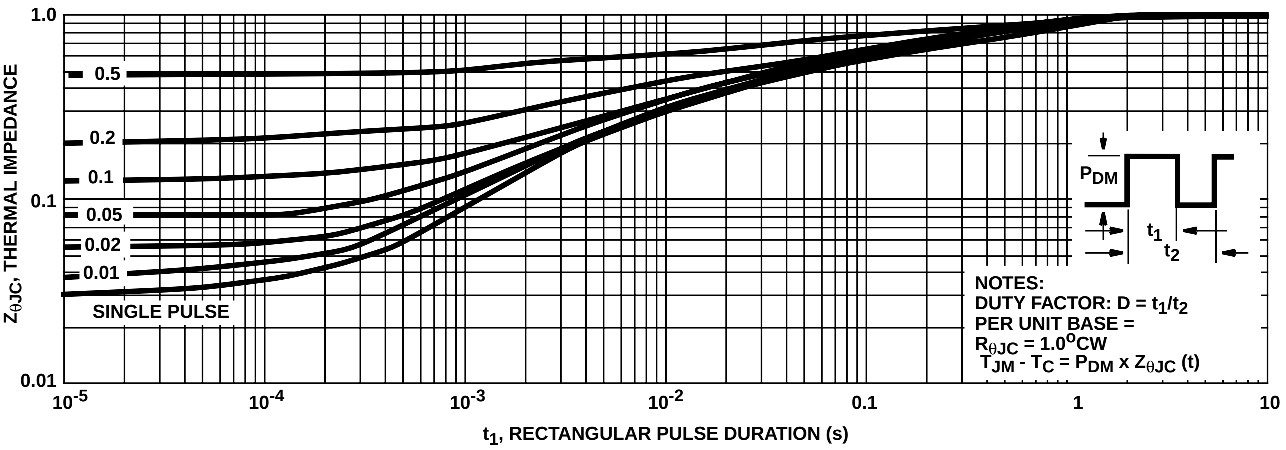


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE



NOTES:
DUTY FACTOR: $D = t_1/t_2$
PER UNIT BASE = $R_{\theta JC} = 1.0^oCW$
$T_{JM} - T_C = P_{DM} \times Z_{\theta JC}(t)$

FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves Unless Otherwise Specified **(Continued)**

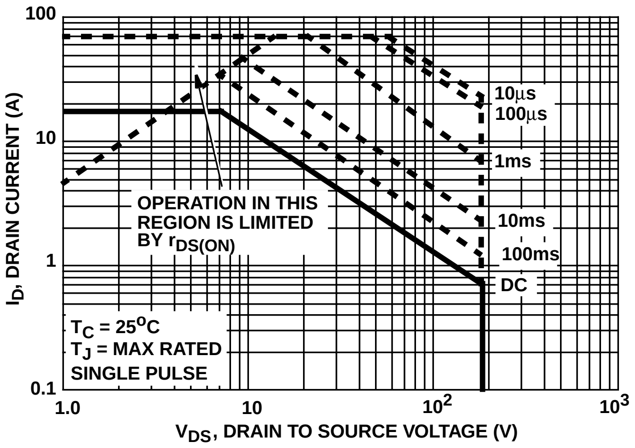


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

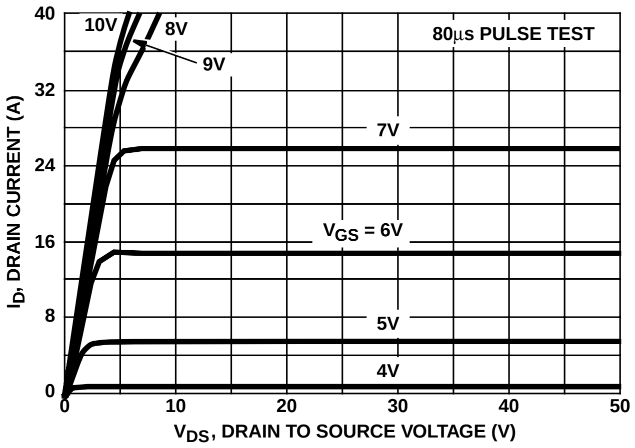


FIGURE 5. OUTPUT CHARACTERISTICS

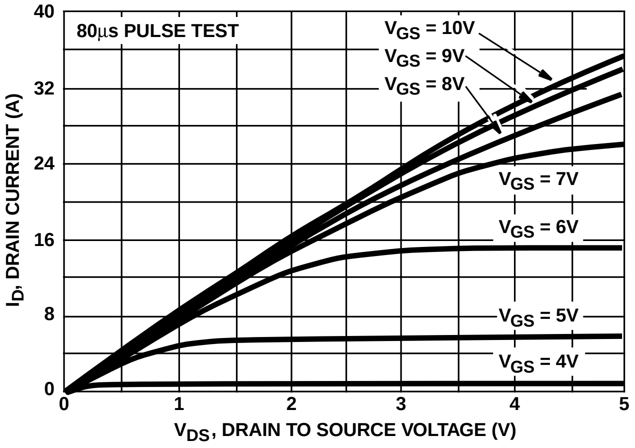


FIGURE 6. SATURATION CHARACTERISTICS

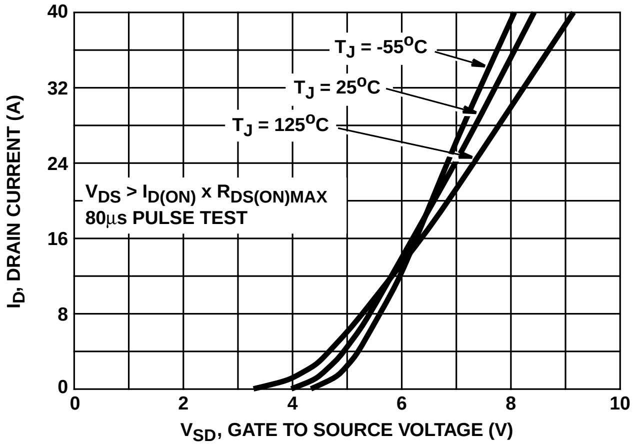
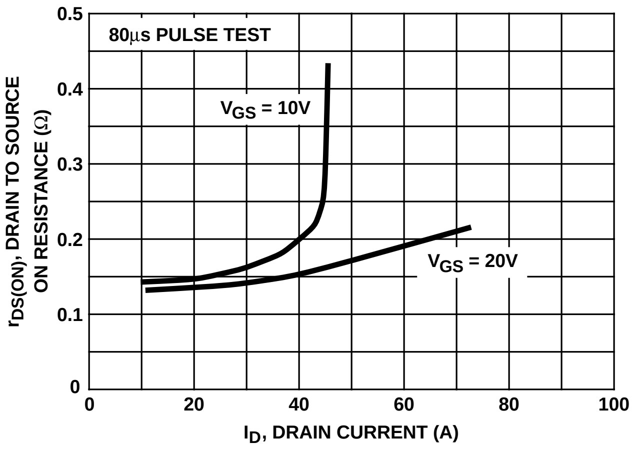


FIGURE 7. TRANSFER CHARACTERISTICS



NOTE: Heating effect of 2µs pulse is minimal.

FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

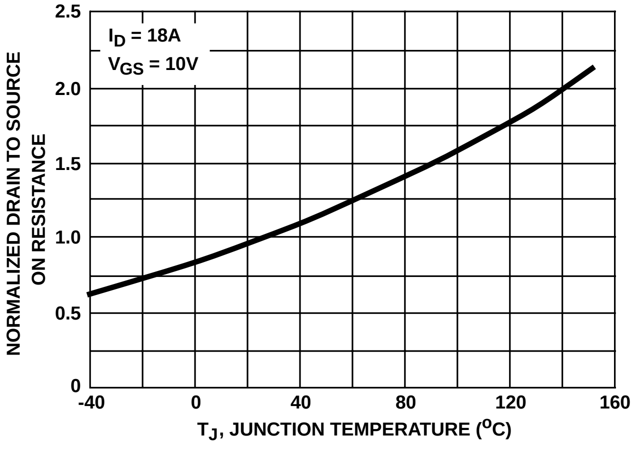


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

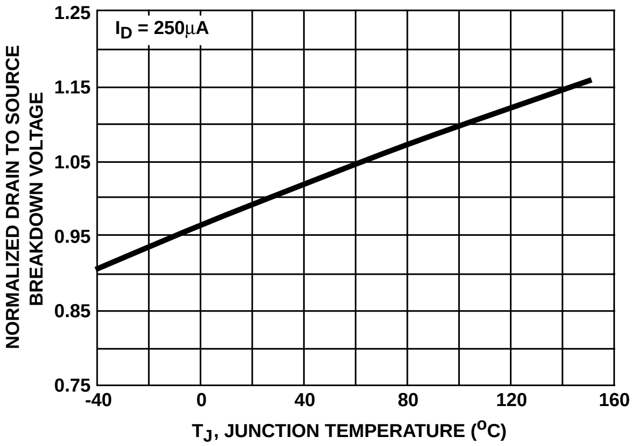


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

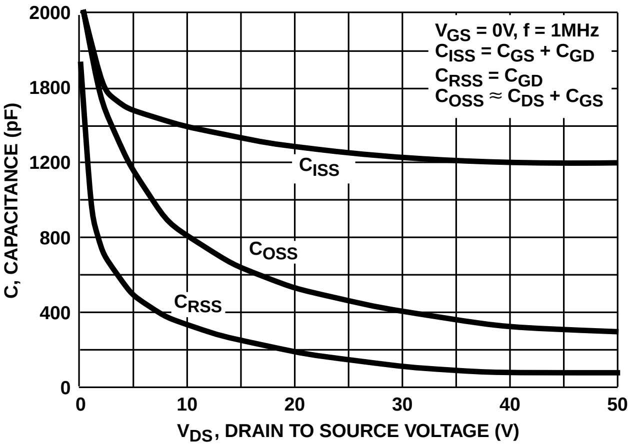


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

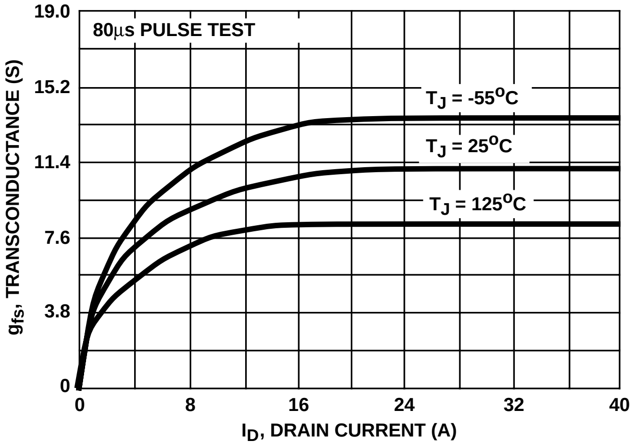


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

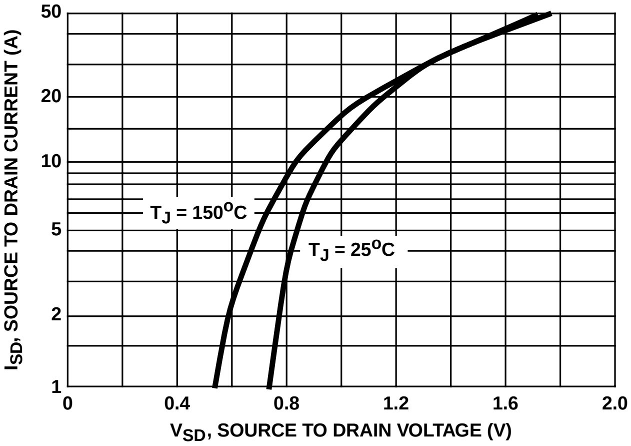


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

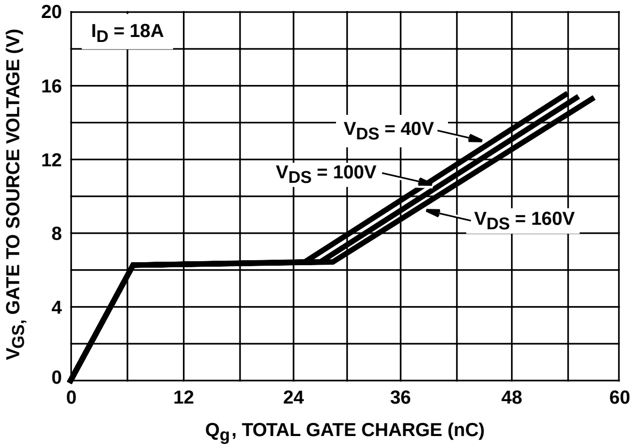


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

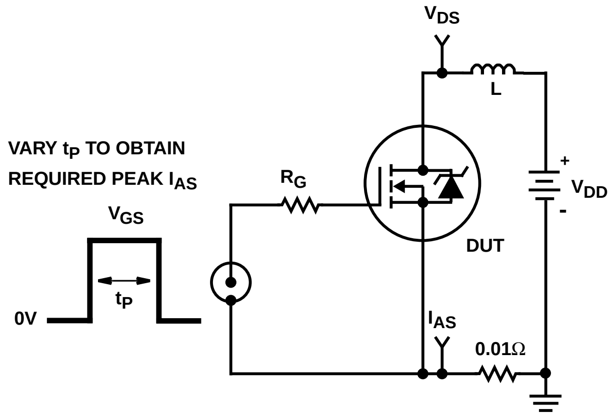


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

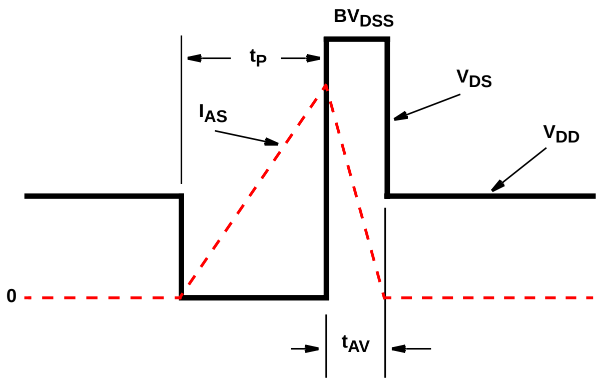


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

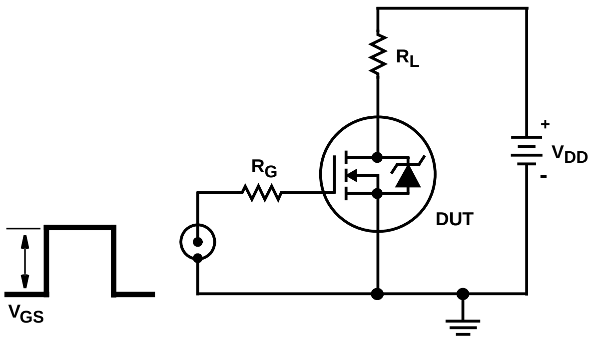


FIGURE 17. SWITCHING TIME TEST CIRCUIT

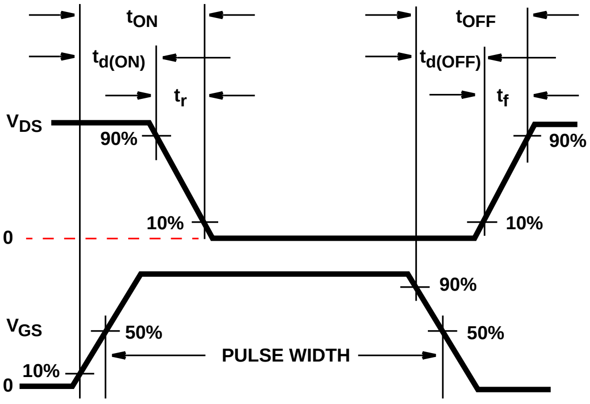


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

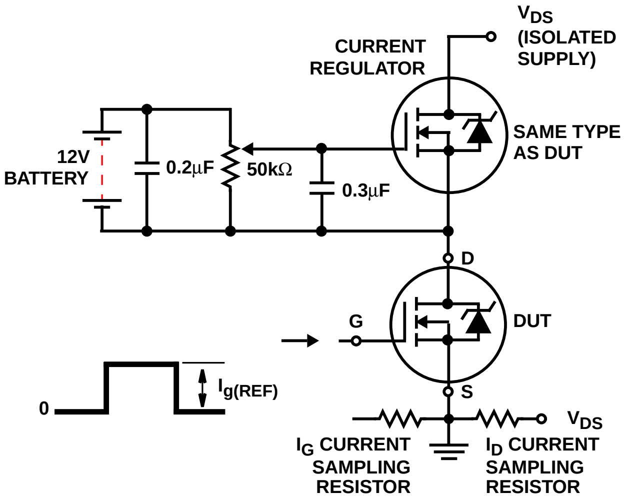


FIGURE 19. GATE CHARGE TEST CIRCUIT

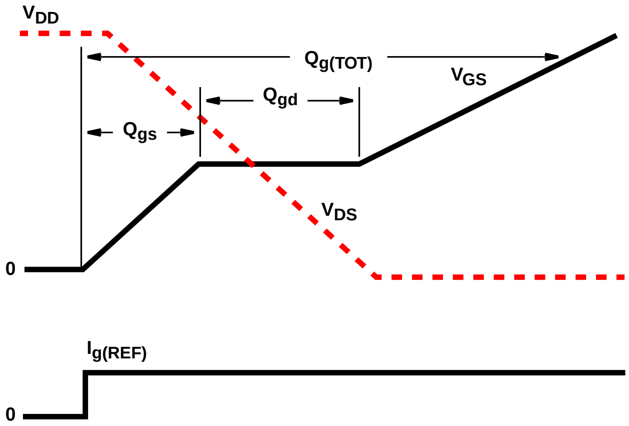


FIGURE 20. GATE CHARGE WAVEFORMS

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