

**12A, 60V, 0.135 Ohm, N-Channel, Logic Level, Power MOSFETs**

These N-Channel logic level ESD protected power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor drivers, relay drivers, and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V to 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

Formerly developmental type TA09861.

**Ordering Information**

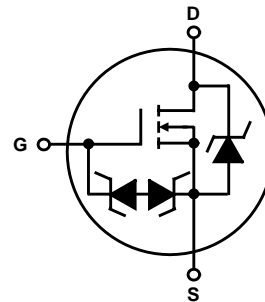
PART NUMBER	PACKAGE	BRAND
RFD12N06RLE	TO-251AA	12N6LE
RFD12N06RLESM	TO-252AA	12N6LE
RFP12N06RLE	TO-220AB	12N06RLE

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in tape and reel, i.e., RFD12N06RLESM9A.

**Features**

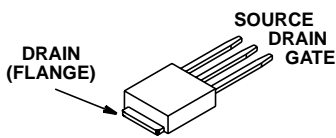
- 12A, 60V
- $r_{DS(ON)} = 0.135\Omega$
- Electrostatic Discharge Protected
- UIS Rating Curve (Single Pulse)
- Design Optimized for 5V Gate Drive
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

**Symbol**

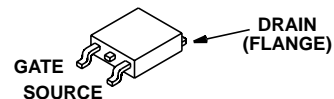


**Packaging**

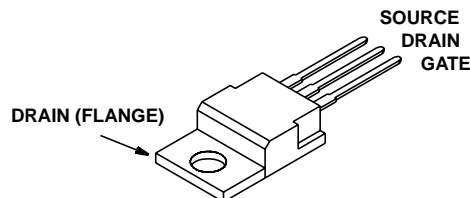
**JEDEC TO-251AA**



**JEDEC TO-252AA**



**JEDEC TO-220AB**



# RFD12N06RLE, RFD12N06RLESM, RFP12N06RLE

## Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

	RFD12N06RLE, RFD12N06RLESM, RFP12N06RLE	UNITS
Drain to Source Voltage (Note 1) . . . . .	60	V
Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) (Note 1) . . . . .	60	V
Continuous Drain Current . . . . .	12	A
Pulsed Drain Current (Note 3) . . . . .	26	A
Gate to Source Voltage . . . . .	-5 to 10	V
Power Dissipation . . . . .	40	W
Linear Derating Factor . . . . .	0.32	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy Rating . . . . .	Refer to UIS SOA Curve	
Electrostatic Discharge Rating ESD, MIL-STD-883, Category B(2)	2	kV
Operating and Storage Temperature . . . . .	-55 to 150	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s . . . . .	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334 . . . . .	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**NOTE:**

1.  $T_J = 25^\circ\text{C}$  to  $125^\circ\text{C}$ .

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	1	-	2	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = \text{Rated } BV_{DSS}$ , $V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$ , $V_{GS} = 0\text{V}$ , $T_C = 150^\circ\text{C}$	-	-	25	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = -5$ to $10\text{V}$	-	-	$\pm 10$	$\mu\text{A}$
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 12\text{A}$ , $V_{GS} = 5\text{V}$ (Figures 7, 8)	-	-	0.135	$\Omega$
		$I_D = 12\text{A}$ , $V_{GS} = 4\text{V}$	-	-	0.160	$\Omega$
Turn-On Time	$t_{(ON)}$	$V_{DD} = 30\text{V}$ , $I_D \approx 6\text{A}$ , $R_L = 5\Omega$ , $R_{GS} = 6.25\Omega$ , $V_{GS} = 5\text{V}$ , (Figures 15, 16)	-	-	60	ns
Turn-On Delay Time	$t_{d(ON)}$		-	12	-	ns
Rise Time	$t_r$		-	20	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	24	-	ns
Fall Time	$t_f$		-	12	-	ns
Turn-Off Time	$t_{(OFF)}$		-	-	-	60
Total Gate Charge	$Q_g(\text{TOT})$	$V_{GS} = 0\text{V}$ to $10\text{V}$	-	-	40	nC
Gate Charge at 5V	$Q_g(5)$	$V_{GS} = 0\text{V}$ to $5\text{V}$				
Threshold Gate Charge	$Q_g(\text{TH})$	$V_{GS} = 0\text{V}$ to $1\text{V}$				
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	3.125	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-251AA and TO-252AA	-	-	100	$^\circ\text{C}/\text{W}$
		TO-220AB	-	-	62	$^\circ\text{C}/\text{W}$

## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = 12\text{A}$	-	-	1.2	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 12\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	200	ns

**NOTES:**

2. Pulse test: pulse width  $\leq 300\text{ms}$ , duty cycle  $\leq 2\%$ .
3. Repetitive rating: pulse width is limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

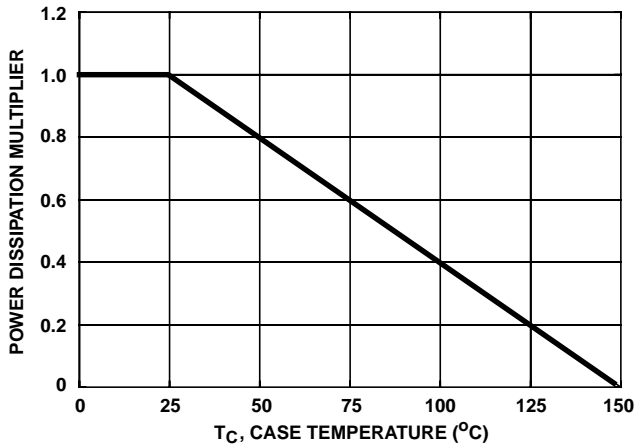


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

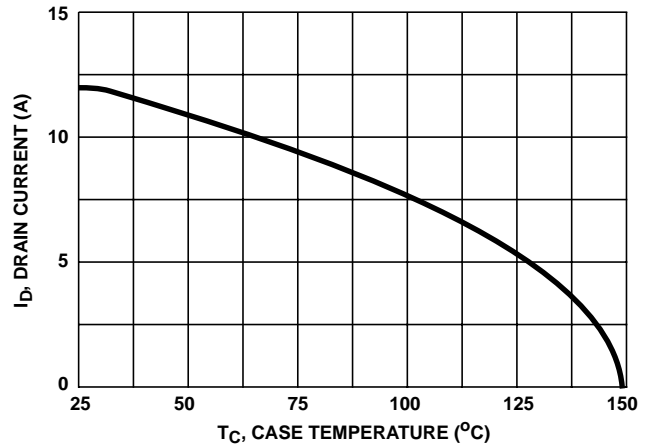


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

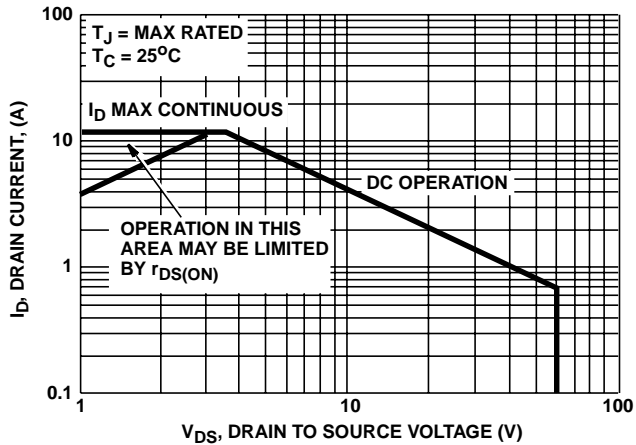
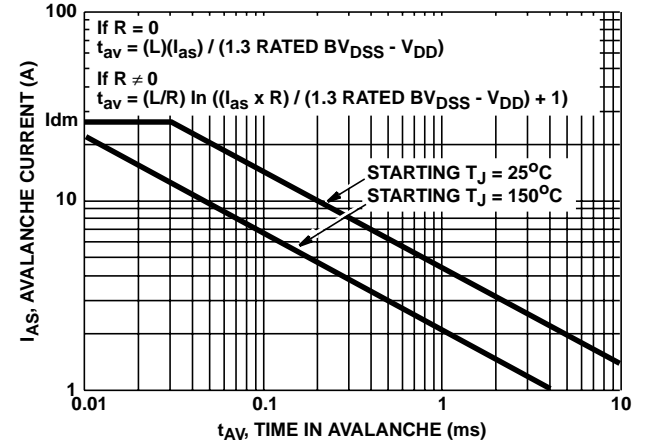


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 4. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

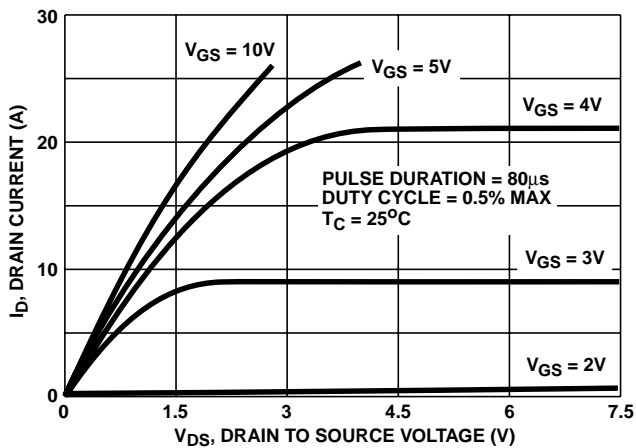


FIGURE 5. SATURATION CHARACTERISTICS

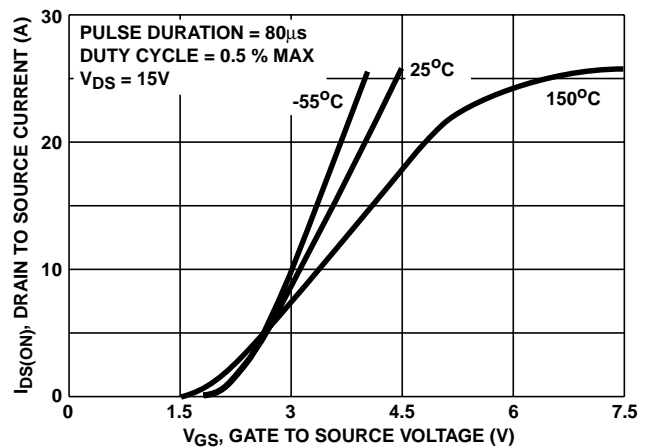


FIGURE 6. TRANSFER CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

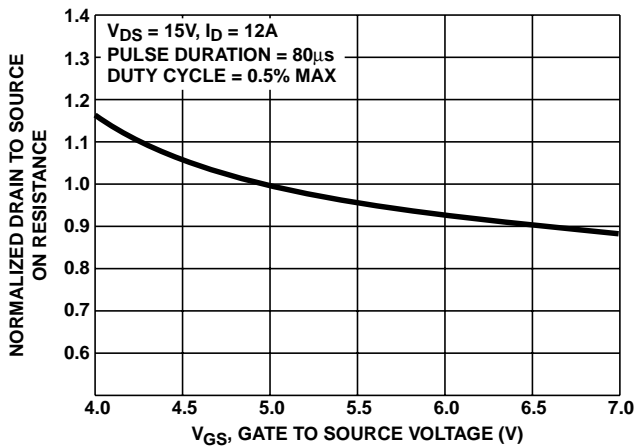


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs GATE TO SOURCE VOLTAGE

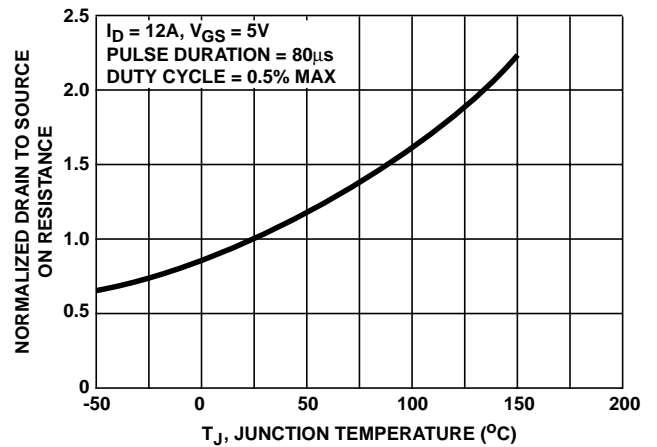


FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

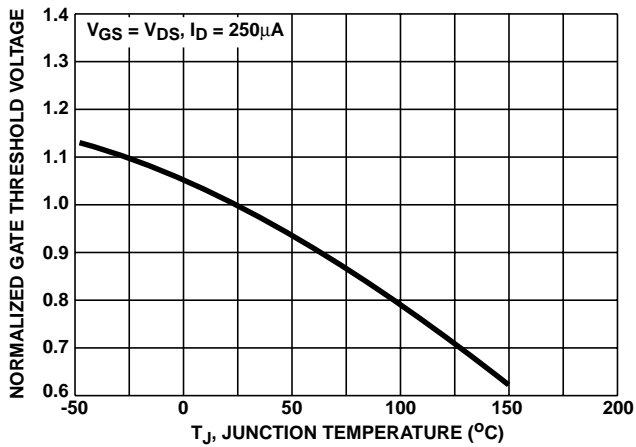


FIGURE 9. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

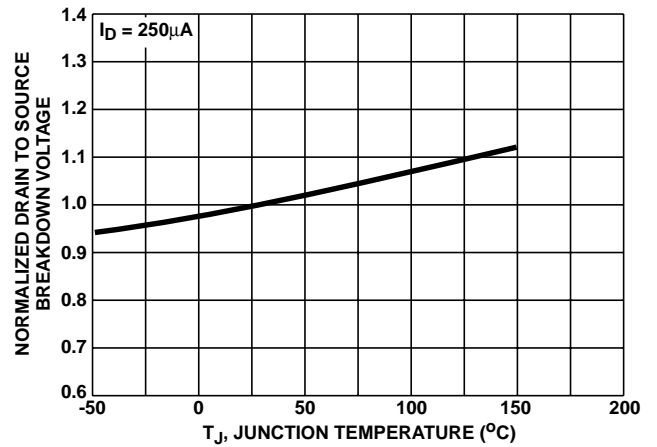


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

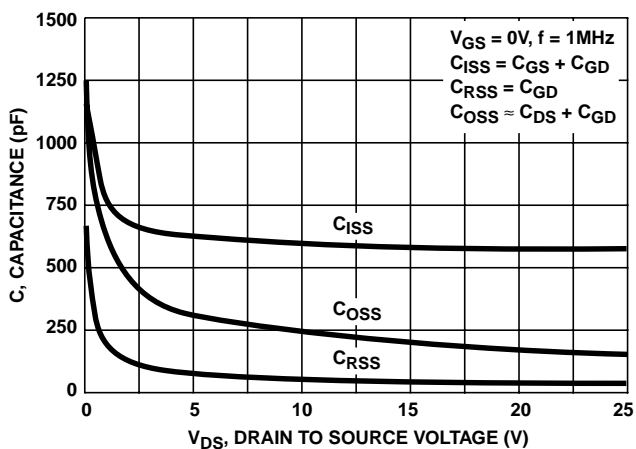
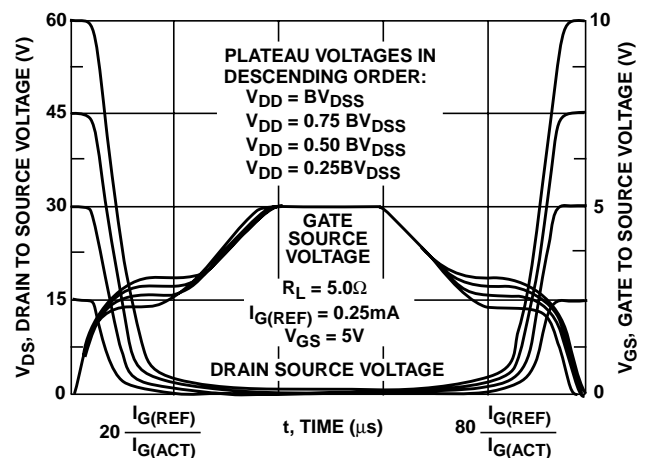


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

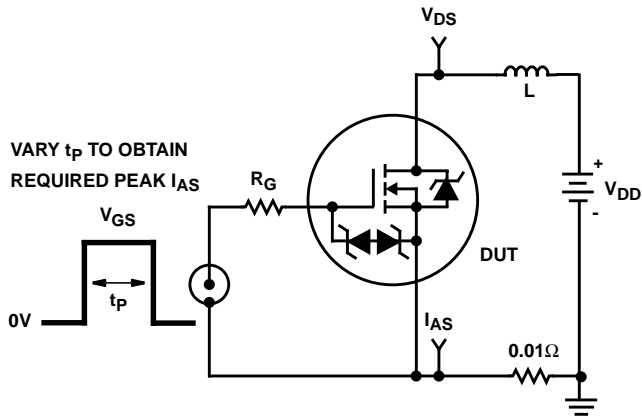


FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT

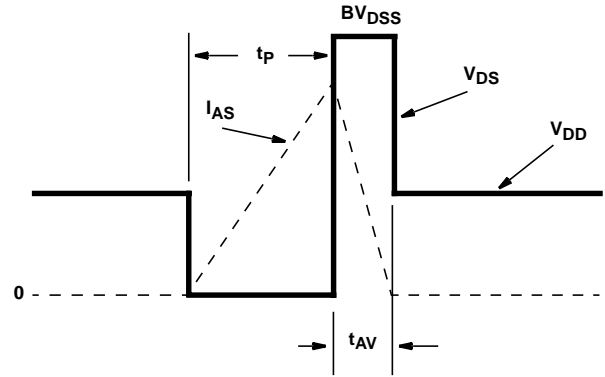


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

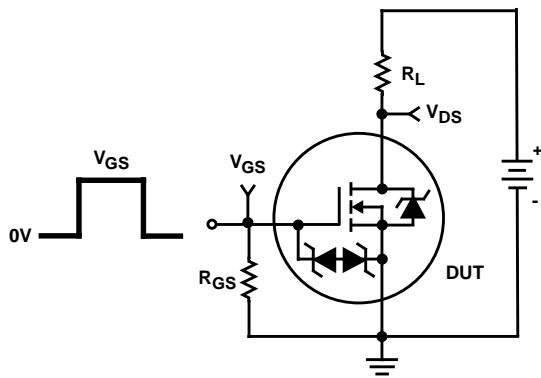


FIGURE 15. SWITCHING TIME TEST CIRCUIT

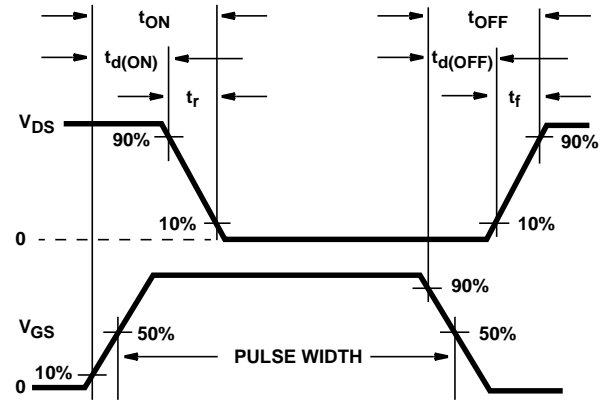


FIGURE 16. RESISTIVE SWITCHING WAVEFORMS

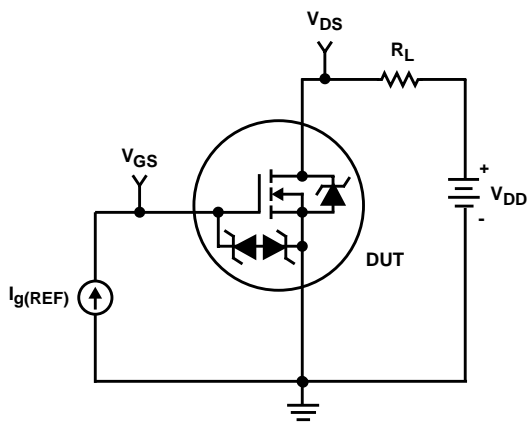


FIGURE 17. GATE CHARGE TEST CIRCUIT

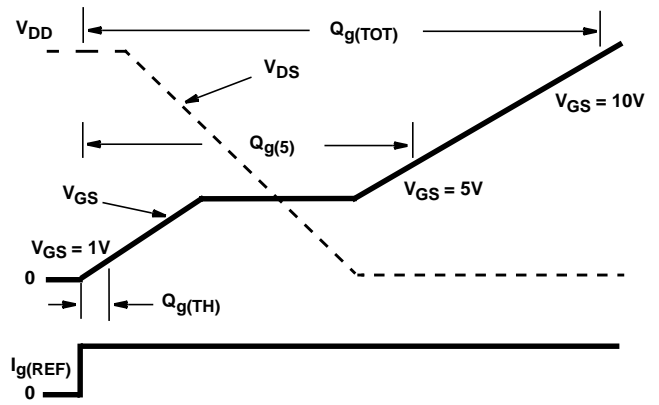


FIGURE 18. GATE CHARGE WAVEFORMS

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