

40A, 100V, 0.040 Ohm, N-Channel Power MOSFETs

These are N-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA9846

Ordering Information

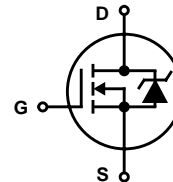
PART NUMBER	PACKAGE	BRAND
RFG40N10	TO-247	RFG40N10
RFP40N10	TO-220AB	RFP40N10
RF1S40N10SM	TO-263AB	F1S40N10

NOTE: When ordering, use the entire part number. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, i.e. RF1S40N10SM9A.

Features

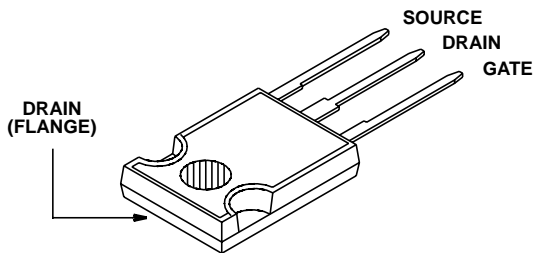
- 40A, 100V
- $r_{DS(ON)} = 0.040\Omega$
- UIS Rating Curve
- SOA is Power Dissipation Limited
- 175°C Operating Temperature
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol

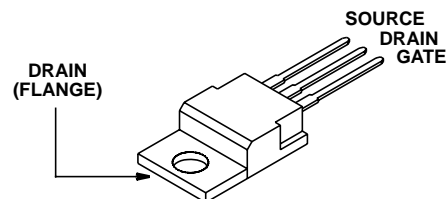


Packaging

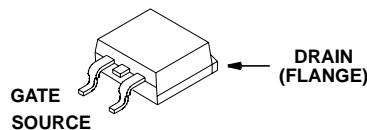
JEDEC STYLE TO-247



JEDEC TO-220AB



JEDEC TO-263AB



RFG40N10, RFP40N10, RF1S40N10SM

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	RFG40N10, RFP40N10, RF1S40N10SM	UNITS
Drain to Source Breakdown Voltage (Note 1)	100	V
Drain to Gate Voltage ($R_{GS} = 1\text{M}\Omega$) (Note 1)	100	V
Gate to Source Voltage	± 20	V
Drain Current		
Continuous (Figure 2)	40	A
Pulsed Drain Current (Note 2)	100	A
Pulsed Avalanche Rating	Figures 4, 12, 13	
Power Dissipation	160	W
Derate Above 25°C	1.07	W/ $^\circ\text{C}$
Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from case for 10s	300	$^\circ\text{C}$
Package Body for 10s, see Techbrief 334	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. $T_J = 25^\circ\text{C}$ to 150°C .
2. Repetitive Rating: pulse width limited by maximum junction temperature.

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$ (Figure 9)	100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$ (Figure 8)	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\text{V}$, $V_{GS} = 0\text{V}$	$T_C = 25^\circ\text{C}$	-	1	μA
			$T_C = 150^\circ\text{C}$	-	50	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 40\text{A}$, $V_{GS} = 10\text{V}$ (Figure 7)	-	-	0.040	Ω
Turn-On Time	t_{ON}	$V_{DD} = 50\text{V}$, $I_D = 20\text{A}$, $R_L = 2.5\Omega$, $V_{GS} = 10\text{V}$, $R_{GS} = 4.2\Omega$ (Figure 11)	-	-	80	ns
Turn-On Delay Time	$t_{d(ON)}$		-	17	-	ns
Rise Time	t_r		-	30	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	42	-	ns
Fall Time	t_f		-	20	-	ns
Turn-Off Time	t_{OFF}		-	-	100	ns
Total Gate Charge	$Q_{g(TOT)}$		$V_{GS} = 0\text{V}$ to 20V	-	-	300
Gate Charge at 10V	$Q_{g(10)}$	$V_{GS} = 0\text{V}$ to 10V	-	-	150	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0\text{V}$ to 2V	-	-	7.5	nC
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	0.94	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-247	-	-	30	$^\circ\text{C}/\text{W}$
		TO-220AB and TO-263AB	-	-	62	$^\circ\text{C}/\text{W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 40\text{A}$	-	-	1.5	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 40\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	200	ns

Typical Performance Curves Unless Otherwise Specified

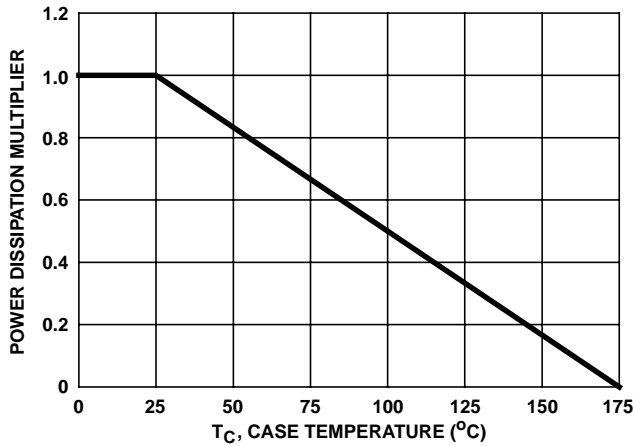


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

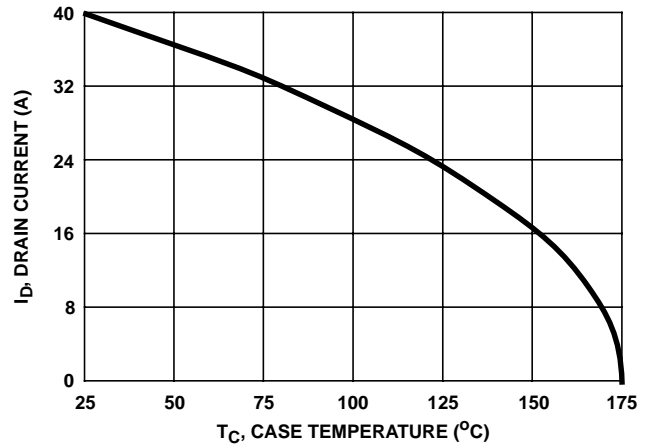


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

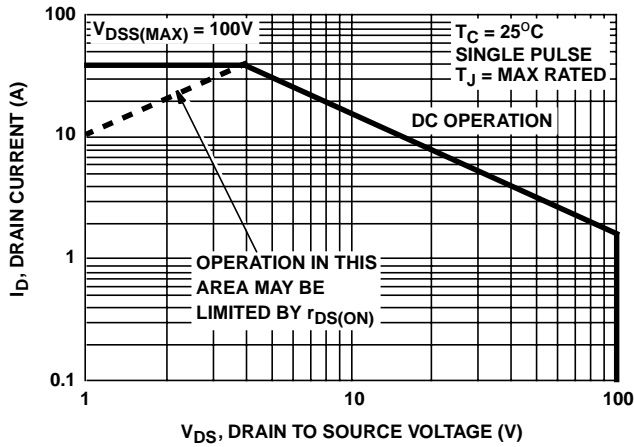
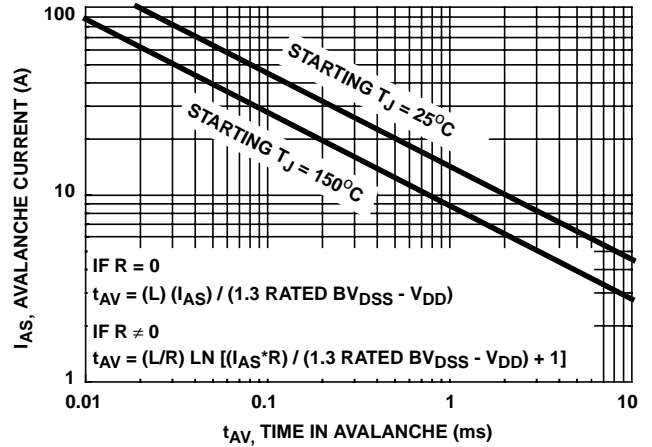


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Intersil application notes AN9321 and AN9322.

FIGURE 4. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

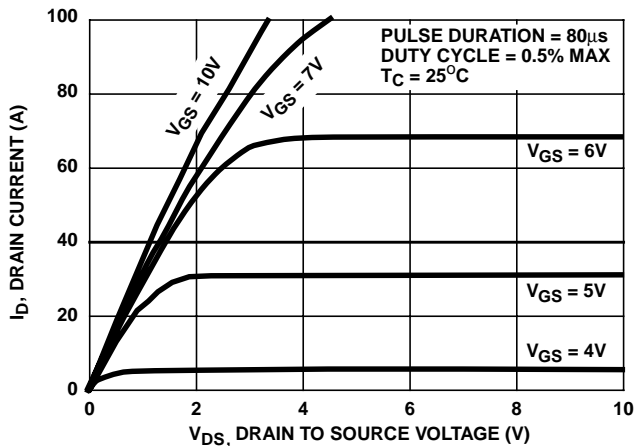


FIGURE 5. SATURATION CHARACTERISTICS

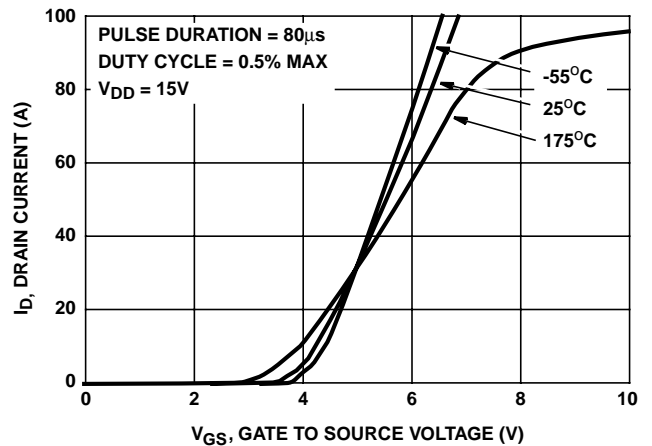


FIGURE 6. TRANSFER CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

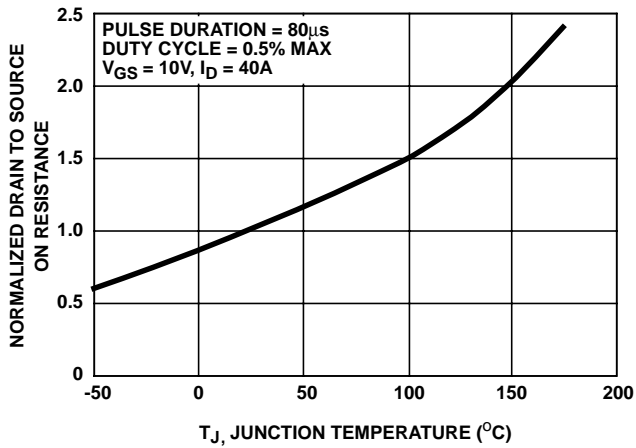


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

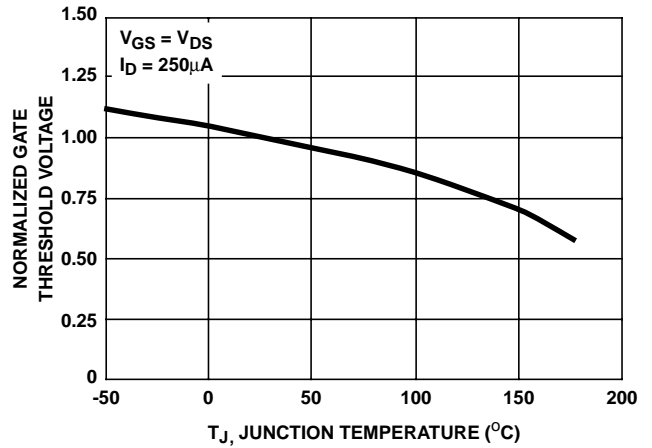


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

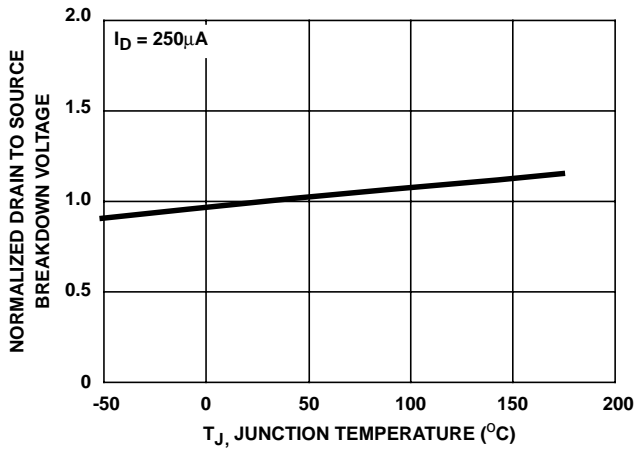


FIGURE 9. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

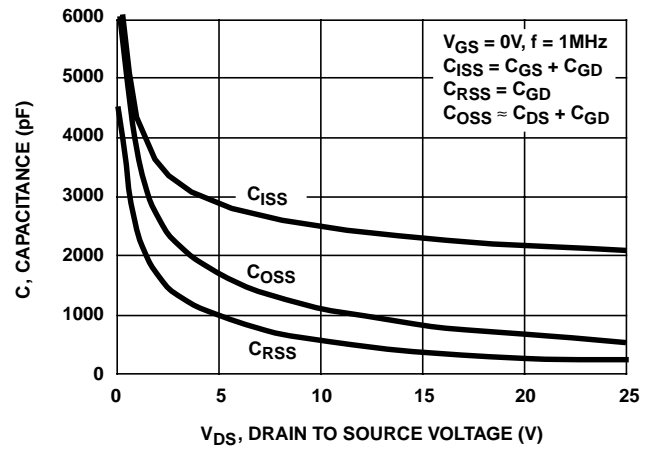
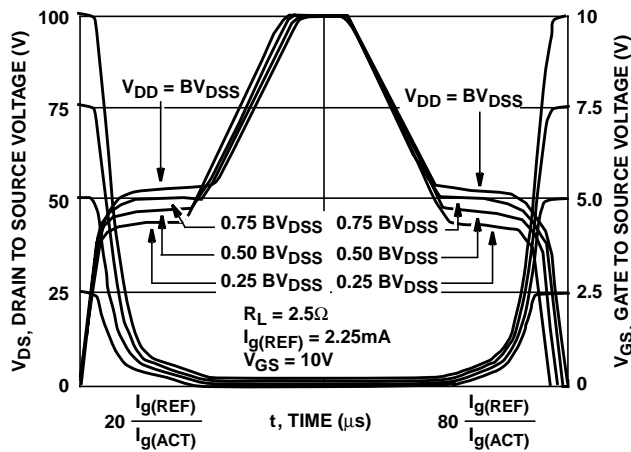


FIGURE 10. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

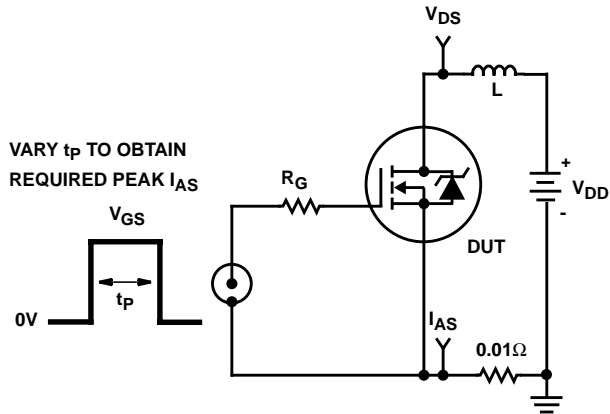


FIGURE 12. UNCLAMPED ENERGY TEST CIRCUIT

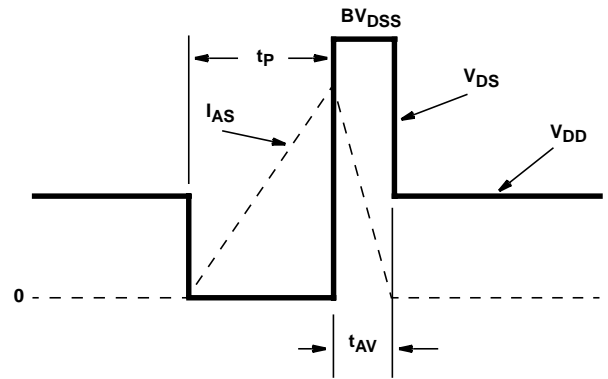


FIGURE 13. UNCLAMPED ENERGY WAVEFORMS

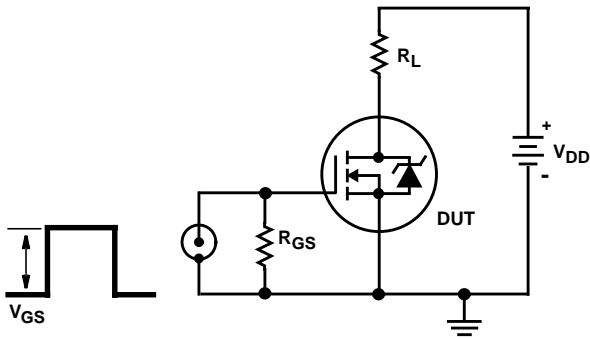


FIGURE 14. SWITCHING TIME TEST CIRCUIT

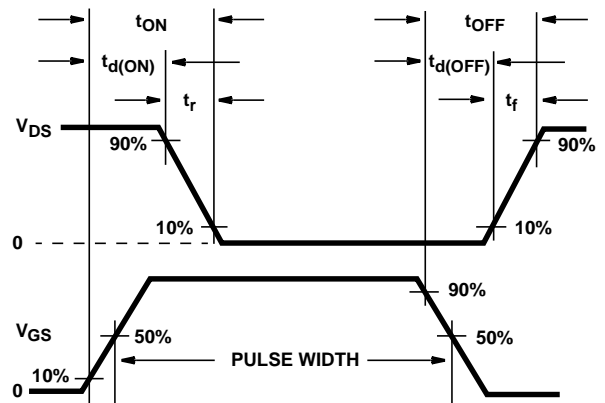


FIGURE 15. RESISTIVE SWITCHING WAVEFORMS

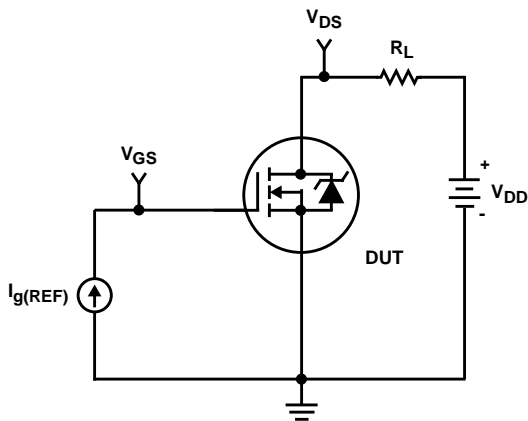


FIGURE 16. GATE CHARGE TEST CIRCUIT

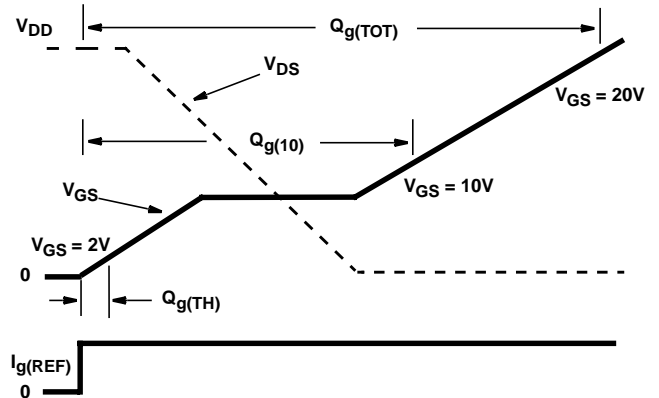


FIGURE 17. GATE CHARGE WAVEFORMS

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

Sales Office Headquarters

NORTH AMERICA

Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE

Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029