

### 4.3A, 1000V, 3.500 Ohm, High Voltage, N-Channel Power MOSFETs

The RFP4N100 and RFP4N100SM are N-Channel enhancement mode silicon gate power field effect transistors. They are designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from an integrated circuit.

Formerly developmental type TA09850.

### Ordering Information

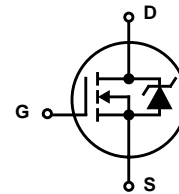
PART NUMBER	PACKAGE	BRAND
RFP4N100	TO-220AB	RFP4N100
RF1S4N100SM	TO-263AB	F1S4N100

NOTE: When ordering, use the entire part number.

### Features

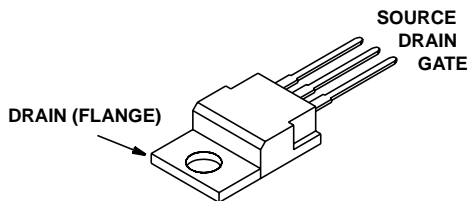
- 4.3A, 1000V
- $r_{DS(ON)} = 3.500\Omega$
- UIS Rating Curve (Single Pulse)
- -55°C to 150°C Operating Temperature
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

### Symbol

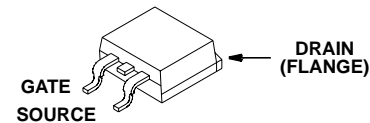


### Packaging

JEDEC TO-220AB



JEDEC TO-263AB



# RFP4N100, RF1S4N100SM

## Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

	RFP4N100, RF1S4N100SM	UNITS
Drain to Source Breakdown Voltage (Note 1) . . . . .	1000	V
Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) (Note 1) . . . . .	1000	V
Continuous Drain Current . . . . .	4.3	A
Pulsed Drain Current (Note 3) . . . . .	17	A
Gate to Source Voltage . . . . .	$\pm 20$	V
Single Pulse Avalanche Rating . . . . .	(See UIS SOA Curve) (Figures 4, 14, 15)	mJ
Maximum Power Dissipation . . . . .	150	W
Linear Derating Factor . . . . .	1.2	W/ $^\circ\text{C}$
Operating and Storage Temperature . . . . .	-55 to 150	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from case for 10s . . . . .	300	$^\circ\text{C}$
Package Body for 10s, see Techbrief 334 . . . . .	260	$^\circ\text{C}$

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**NOTE:**

1.  $T_J = 25^\circ\text{C}$  to  $125^\circ\text{C}$ .

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$ (Figure 10)	1000	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	2	-	4	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 1000\text{V}$ , $V_{GS} = 0\text{V}$	-	-	25	$\mu\text{A}$
		$V_{DS} = 800\text{V}$ , $V_{GS} = 0\text{V}$ , $T_C = 150^\circ\text{C}$	-	-	100	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 2.5\text{A}$ , $V_{GS} = 10\text{V}$ (Figures 8, 9)	-	-	3.500	$\Omega$
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 500\text{V}$ , $I_D \approx 3.9\text{A}$ , $R_{GS} = 9.1\Omega$ , $R_L = 120\Omega$	-	-	30	ns
Rise Time	$t_r$		-	-	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	-	170	ns
Fall Time	$t_f$		-	-	50	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	$V_{GS} = 20\text{V}$ , $I_D = 3.9\text{A}$ , $V_{DS} = 800\text{V}$ (Figure 13)	-	-	120	nC
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	0.83	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		-	-	62	$^\circ\text{C}/\text{W}$

## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = 4.3\text{A}$	-	-	1.8	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 3.9\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	1000	ns

**NOTES:**

2. Pulse test: pulse width  $\leq 80\mu\text{s}$ , duty cycle  $\leq 2\%$ .
3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves  $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

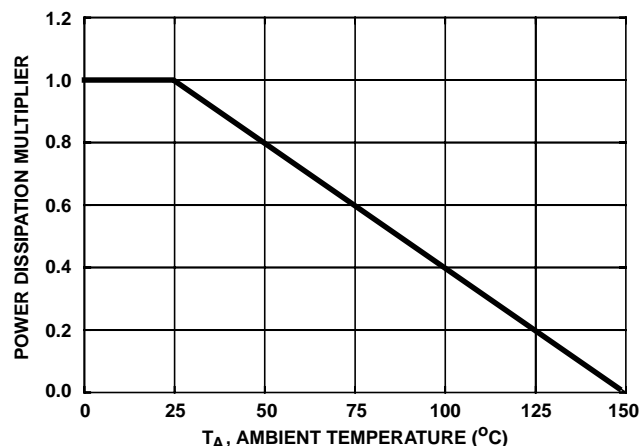


FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

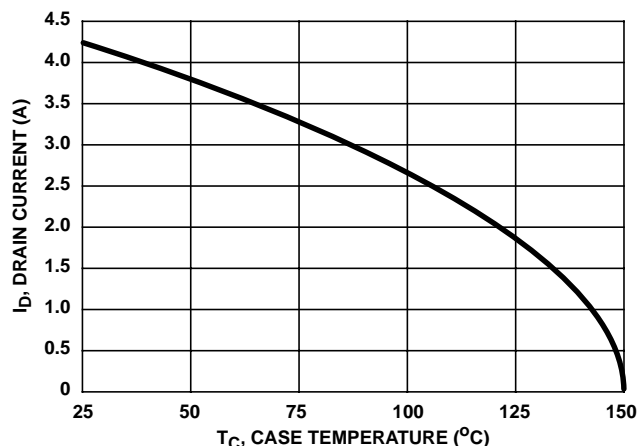


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

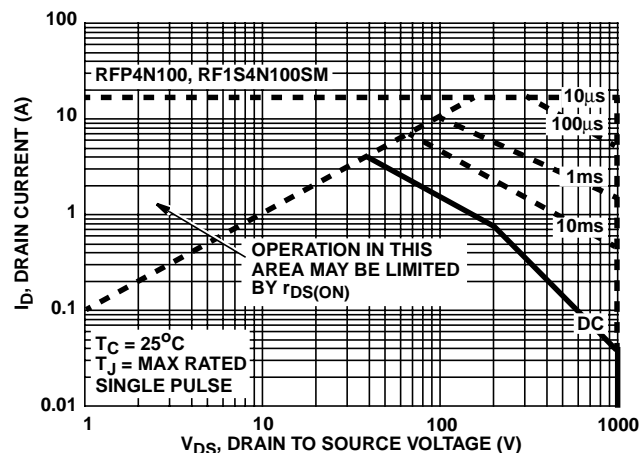


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

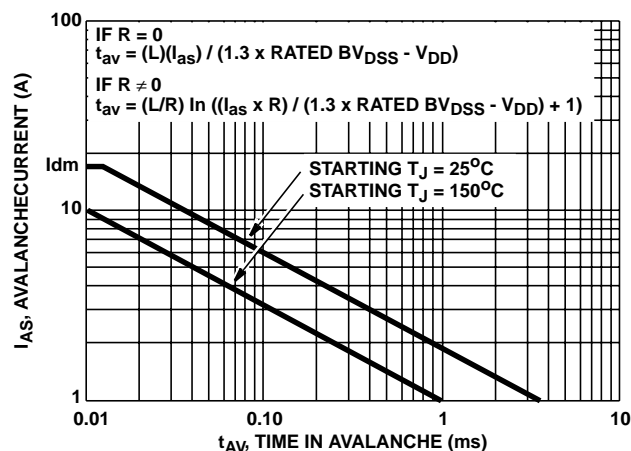


FIGURE 4. UNCLAMPED INDUCTIVE SWITCHING SOA

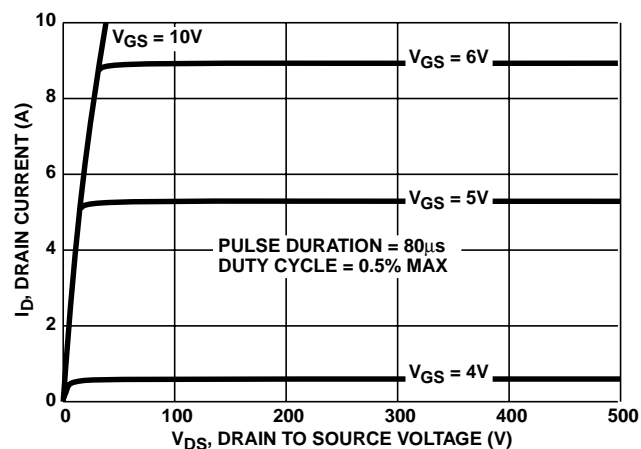


FIGURE 5. OUTPUT CHARACTERISTICS

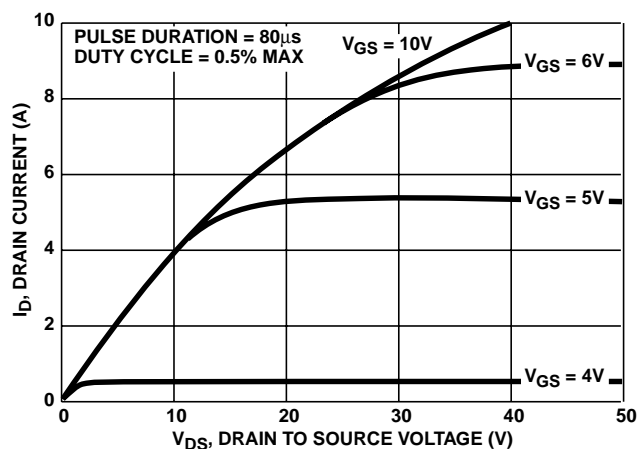


FIGURE 6. SATURATION CHARACTERISTICS

Typical Performance Curves  $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified (Continued)

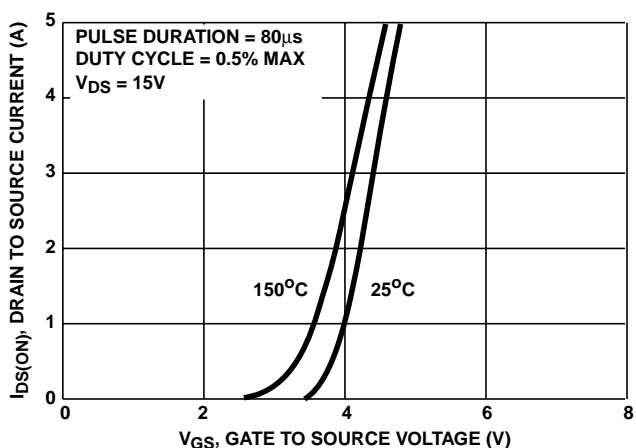


FIGURE 7. TRANSFER CHARACTERISTICS

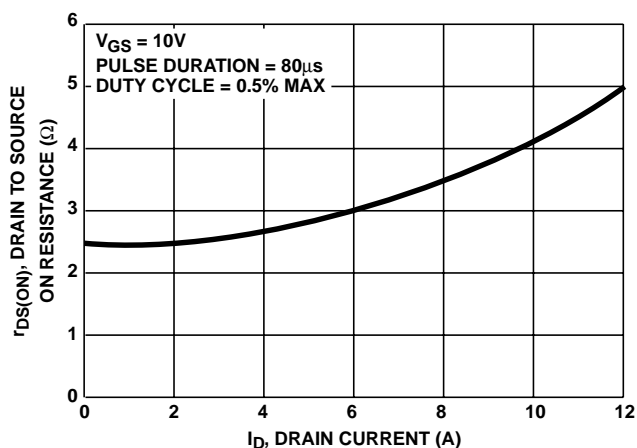


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

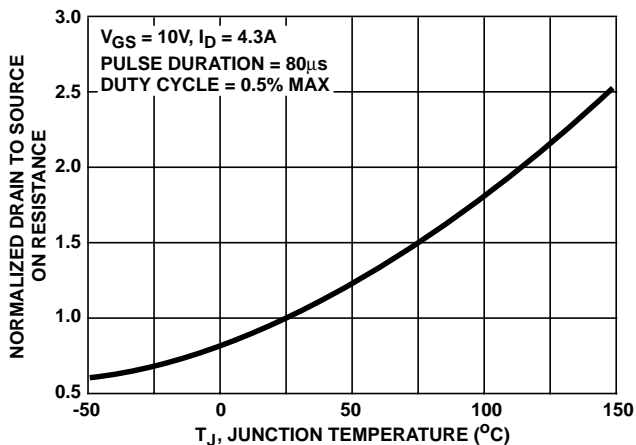


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

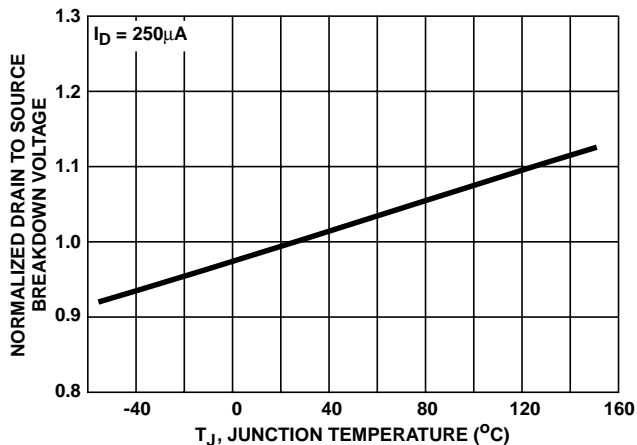


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

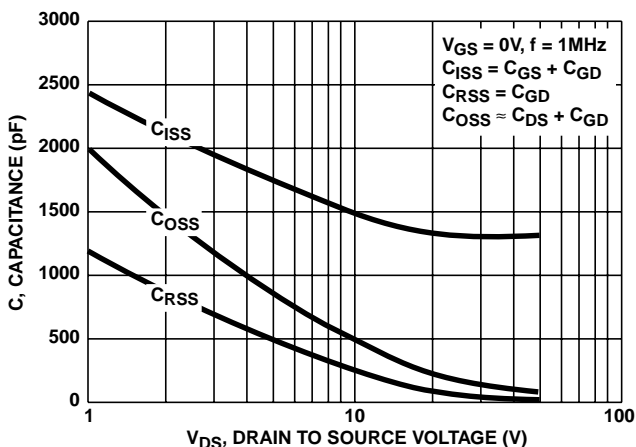


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

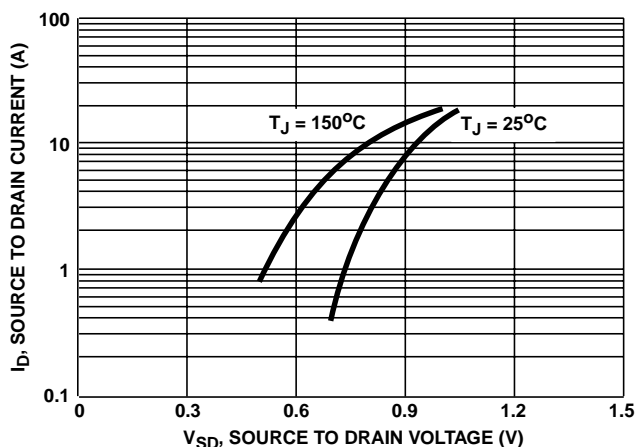


FIGURE 12. DRAIN CURRENT vs SOURCE TO DRAIN DIODE VOLTAGE

Typical Performance Curves  $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified (Continued)

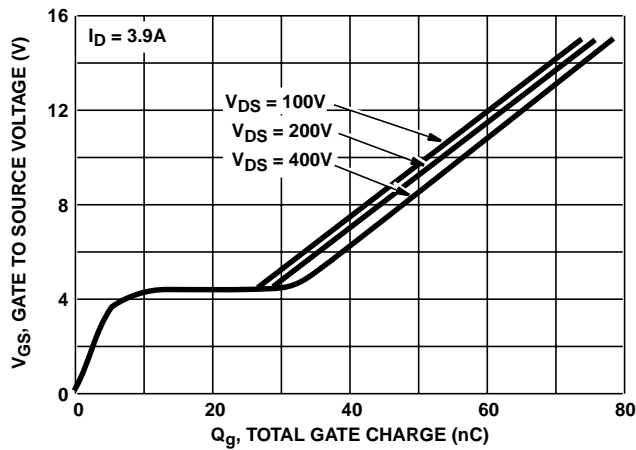


FIGURE 13. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

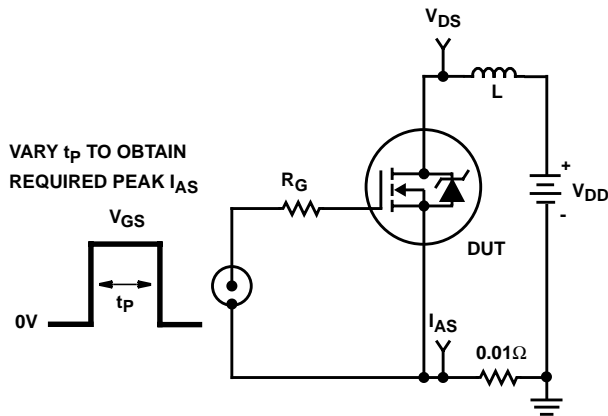


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

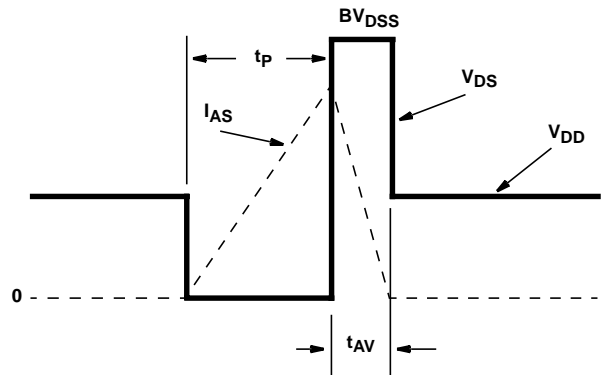


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

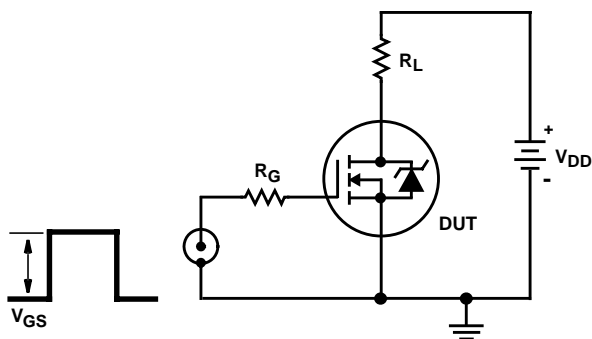


FIGURE 16. SWITCHING TIME TEST CIRCUIT

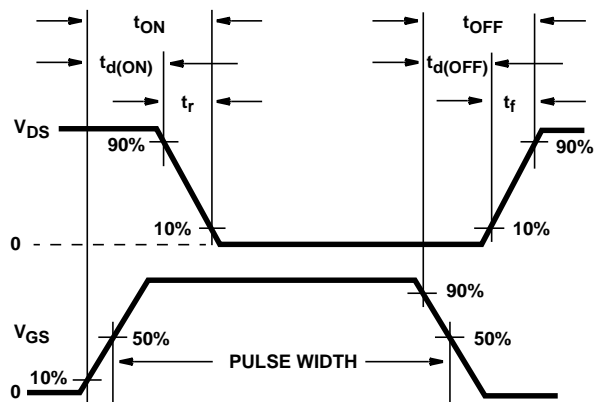


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

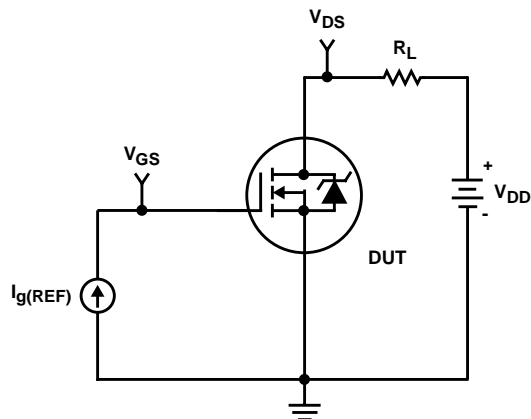


FIGURE 18. GATE CHARGE TEST CIRCUIT

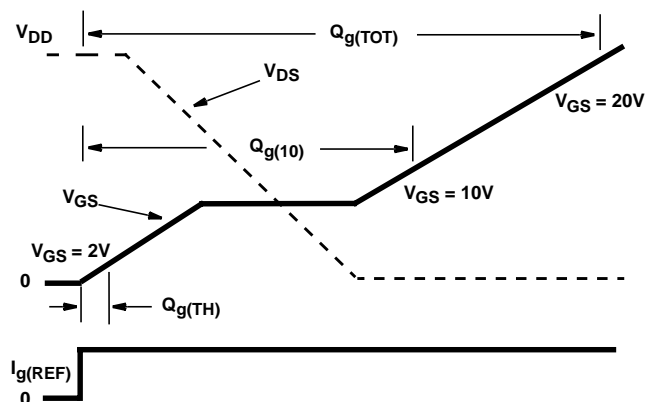


FIGURE 19. GATE CHARGE WAVEFORMS

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