

Multilevel Pipeline Registers

These devices are multilevel pipeline registers implemented using a low power CMOS process. They are pin for pin compatible replacements for industry standard multilevel pipeline registers such as the L29C520 and L29C521. The HSP9520 and HSP9521 are direct replacements for the AM29520 and AM29521 and WS59520 and WS59521.

They consist of four 8-bit registers which are dual ported. They can be configured as a single four level pipeline or a dual two level pipeline. A single 8-bit input is provided, and the pipelining configuration is determined by the instruction code input to the I0 and I1 inputs (see instruction control).

The contents of any of the four registers is selectable at the multiplexed outputs through the use of the S0 and S1 multiplexer control inputs (see register select. The output is 8 bits wide and is three-stated through the use of the OE input.

The HSP9520 and HSP9521 differ only in the way data is loaded into and between the registers in dual two-level operation. In the HSP9520 when data is loaded into the first level the existing data in the first level is moved to the second level. In the HSP9521 loading the first level simply causes the current data to be overwritten. Transfer of data to the second level is achieved using the single four level mode (I1, I0 = '0'). This instruction also causes the first level to be loaded. The HOLD instruction (I1, I0 = '1') provides a means of holding the contents of all registers.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HSP9520CP	0 to 70	24 Ld PDIP	E24.3
HSP9520CS	0 to 70	24 Ld SOIC	M24.3
HSP9521CP	0 to 70	24 Ld PDIP	E24.3
HSP9521CS	0 to 70	24 Ld SOIC	M24.3

Features

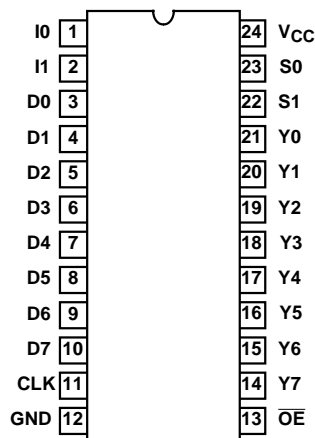
- Four 8-Bit Registers
- Hold, Transfer and Load Instructions
- Single 4-Stage or Dual-2 Stage Pipelining
- All Register Contents Available at Output
- Fully TTL Compatible
- Three-State Outputs
- High Speed, Low Power CMOS

Applications

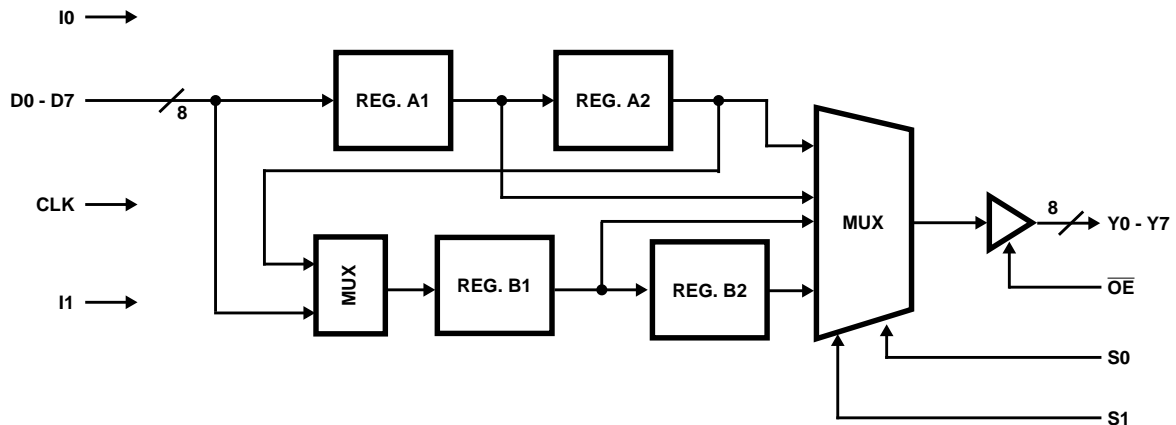
- Array Processor
- Digital Signal Processor
- A/D Buffer
- Telecommunication
- Byte Wide Shift Register
- Mainframe Computers

Pinout

HSP9520, HSP9521 (SOIC, PDIP)
TOP VIEW



Block Diagram



Pin Descriptions

NAME	DIP PIN	TYPE	DESCRIPTION
V _{CC}	24		The +5V Power Supply Pin. A 0.1μF capacitor between the V _{CC} and GND pin is recommended.
GND	12		The device ground.
CLK	11	I	Input Clock. Data is latched on the low to high transition of this clock signal. Input setup and hold times with respect to the clock must be met for proper operation.
D0-7	3-10	I	Data Input Port. These inputs are used to supply the 8 bits of data which will be latched into the selected register on the next rising clock edge.
Y0-7	21-14	O	Data Output Port. This 8-bit port provides the output data from the four internal registers. They are provided in a multiplexed fashion, and are controlled via the multiplexer control inputs (S0 and S1).
I0, I1	1, 2	I	Instruction Control Inputs. These inputs are used to provide the instruction code which determines the internal register pipeline configuration. Refer to the Instruction Control Table for the specific codes and their associated configurations.
S0, S1	23, 22	I	Multiplexer Control Inputs. These inputs select which of the four internal registers contents will be available at the output port. Refer to the Register Select Table for the codes to select each register.
\overline{OE}	13	I	Output Enable. This input controls the state of the output port (Y0 - Y7). A LOW on this control line enables the port for output. When \overline{OE} is HIGH, the output drivers are in the high impedance state. Internal latching or transfer of data is not affected by this pin.

HSP9520, HSP9521

Absolute Maximum Ratings

Supply Voltage +8.0V
 Input or Output Voltage Applied GND -0.5 to V_{CC} +0.5V

Operating Conditions

Voltage Range -4.75V to 5.25V
 Temperature Range 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
 PDIP Package 67
 SOIC Package 77.0
 Maximum Junction Temperature 150°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications V_{CC} = 5.0V ±5%, T_A = 0°C to 70°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Logical One Input Voltage	V _{IH}	V _{CC} = 5.25V	2.0	-	V
Logical Zero Input Voltage	V _{IL}	V _{CC} = 4.75V	-	0.8	V
Output HIGH Voltage	V _{OH}	I _{OH} = -6.5mA, V _{CC} = 4.75V	2.4	-	V
Output LOW Voltage	V _{OL}	I _{OH} = +20.0mA, V _{CC} = 4.75V	-	0.5	V
Input Leakage Current	I _I	V _{IN} = V _{CC} or GND, V _{CC} = 5.25V	-10	-10	μA
Output Leakage Current	I _O	V _{OUT} = V _{CC} or GND, V _{CC} = 5.25V	-10	-10	μA
Standby Power Supply Current	I _{CCSB}	V _{IN} = V _{CC} or GND, V _{CC} = 5.25V Outputs Open	-	500	μA
Operating Power Supply Current	I _{CCOP}	f = 5.0MHz, V _{IN} = V _{CC} or GND, V _{CC} = 5.25V, Outputs Open (Note 2)	-	12	mA
Input Capacitance	C _{IN}	FREQ = 1MHZ, V _{CC} = Open, All Measurements are Referenced to Device Ground	-	12	pF
Output Capacitance	C _O		-	12	pF

AC Electrical Specifications V_{CC} = 5.0V ±5%, T_A = 0°C to 70°C (Note 3)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Clock to Data Out	t _{PD}		-	21	ns
Mux Select to Data Out	t _{SELD}		-	20	ns
Input Setup Time (DO-7/10-7)	t _S		10	-	ns
Input Hold Time (DO-7/10-7)	t _H		3	-	ns
Output Enable Time	t _{ENA}		-	20	ns
Output Disable Time	t _{DIS}	(Note 4)	-	13	ns
Clock Pulse Width	t _{PW}		10	-	ns

NOTES:

2. Power supply current is proportional to frequency. Typical rating for I_{CCOP} is 2.4mA/MHz.
3. AC Testing is performed as follows: Input levels: 0V and 3.0V, timing reference levels = 1.5V, input rise and fall times driven at 1ns/V, output load C_L = 40pF.
4. Controlled by design or process parameters and not directly tested. Characterized upon initial design and after major design and/or process changes.

Timing Waveform

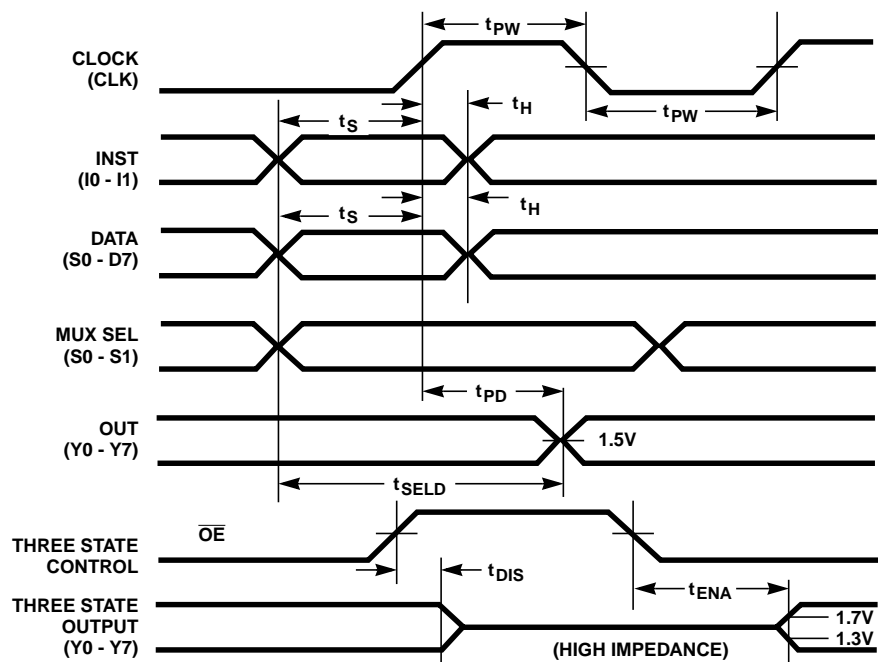


TABLE 1. INSTRUCTION CONTROL

I1	I0	HSP9520	HSP9521
0	0		
0	1		
1	0		
1	1	All Registers Hold	All Registers Hold

TABLE 2. REGISTER SELECT

S1	S0	HSP9520 OR HSP9521
0	0	B2
0	1	B1
1	0	A2
1	1	A1

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