Data Sheet May 1999 File Number 2945.7

850MHz, Low Distortion Current Feedback Operational Amplifiers

The HFA1100, 1120 are a family of high-speed, wideband, fast settling current feedback amplifiers built with Intersil's proprietary complementary bipolar UHF-1 process. Both amplifiers operate with single supply voltages as low as 4.5V (see Application Information section).

The HFA1100 is a basic op amp with uncommitted pins 1, 5, and 8. The HFA1120 includes inverting input bias current adjust pins (pins 1 and 5) for adjusting the output offset voltage.

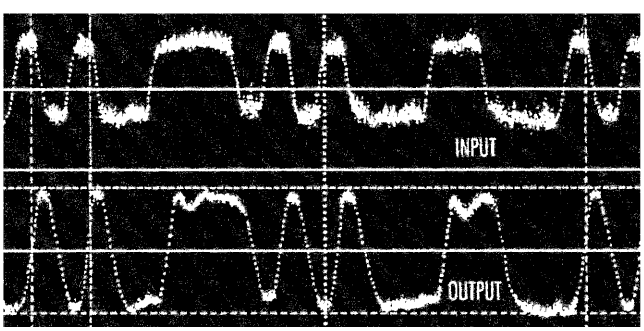
These devices offer a significant performance improvement over the AD811, AD9617/18, the CLC400-409, and the EL2070, EL2073, EL2030.

For Military grade product refer to the HFA1100/883, HFA1120/883 data sheet.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HFA1100IP	-40 to 85	8 Ld PDIP	E8.3
HFA1100IB (H1100I)	-40 to 85	8 Ld SOIC	M8.15
HFA1120IB (H1120I)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	DIP Evaluation Board for High-Speed Op Amps		

The Op Amps with Fastest Edges



INPUT 220MHz SIGNAL

OUTPUT (A_V = 2) HFA1130 OP AMP

0ns 25ns

Features

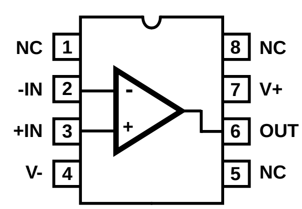
- Low Distortion (30MHz, HD2). . . . . -56dBc
- -3dB Bandwidth 850MHz
- Very Fast Slew Rate 2300V/µs
- Fast Settling Time (0.1%) 11ns
- Excellent Gain Flatness
  - (100MHz) . . . . ±0.14dB
  - (50MHz) . . . . ±0.04dB
- High Output Current 60mA
- Overdrive Recovery . . . . <10ns
- Operates with 5V Single Supply (See AN9745)

Applications

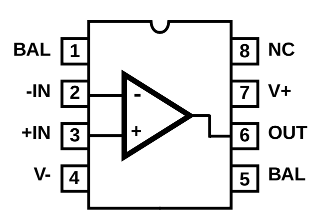
- Video Switching and Routing
- Pulse and Video Amplifiers
- RF/IF Signal Processing
- Flash A/D Driver
- Medical Imaging Systems
- Related Literature
  - AN9420, Current Feedback Theory
  - AN9202, HFA11XX Evaluation Fixture
  - AN9745, Single 5V Supply Operation

Pinouts

HFA1100
(PDIP, SOIC)
TOP VIEW



HFA1120
(SOIC)
TOP VIEW



Absolute Maximum Ratings $T_A = 25^oC$

Voltage Between V+ and V- 12V
Input Voltage . . . . V_{SUPPLY}
Differential Input Voltage 5V
Output Current (50% Duty Cycle) 60mA

Operating Conditions

Temperature Range . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^oC/W)	θ_{JC} (^oC/W)
PDIP Package	130	N/A
SOIC Package	170	N/A

Maximum Junction Temperature (Plastic Package) . . . . 150^oC
Maximum Storage Temperature Range . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 2) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage (Note 3)		A	25	-	2	6	mV
		A	Full	-	-	10	mV
Input Offset Voltage Drift		C	Full	-	10	-	$\mu V/^oC$
V_{IO} CMRR	$\Delta V_{CM} = \pm2V$	A	25	40	46	-	dB
		A	Full	38	-	-	dB
V_{IO} PSRR	$\Delta V_S = \pm1.25V$	A	25	45	50	-	dB
		A	Full	42	-	-	dB
Non-Inverting Input Bias Current (Note 3)	+IN = 0V	A	25	-	25	40	μA
		A	Full	-	-	65	μA
$+I_{BIAS}$ Drift		C	Full	-	40	-	$nA/^oC$
$+I_{BIAS}$ CMS	$\Delta V_{CM} = \pm2V$	A	25	-	20	40	μA/V
		A	Full	-	-	50	μA/V
Inverting Input Bias Current (Note 3)	-IN = 0V	A	25	-	12	50	μA
		A	Full	-	-	60	μA
$-I_{BIAS}$ Drift		C	Full	-	40	-	$nA/^oC$
$-I_{BIAS}$ CMS	$\Delta V_{CM} = \pm2V$	A	25	-	1	7	μA/V
		A	Full	-	-	10	μA/V
$-I_{BIAS}$ PSS	$\Delta V_S = \pm1.25V$	A	25	-	6	15	μA/V
		A	Full	-	-	27	μA/V
$-I_{BIAS}$ Adj. Range (HFA1120)		A	25	±100	±200	-	μA
Non-Inverting Input Resistance		A	25	25	50	-	kΩ
Inverting Input Resistance		C	25	-	20	30	Ω
Input Capacitance (Either Input)		B	25	-	2	-	pF
Input Common Mode Range		C	Full	±2.5	±3.0	-	V
Input Noise Voltage (Note 3)	100kHz	B	25	-	4	-	$nV/\sqrt{Hz}$
+Input Noise Current (Note 3)	100kHz	B	25	-	18	-	$pA/\sqrt{Hz}$
-Input Noise Current (Note 3)	100kHz	B	25	-	21	-	$pA/\sqrt{Hz}$

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 2) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS A_V = +2, Unless Otherwise Specified							
Open Loop Transimpedance (Note 3)		B	25	-	300	-	kΩ
-3dB Bandwidth (Note 3)	V_{OUT} = 0.2V_{P-P}, A_V = +1	B	25	530	850	-	MHz
-3dB Bandwidth	V_{OUT} = 0.2V_{P-P}, A_V = +2, R_F = 360Ω	B	25	-	670	-	MHz
Full Power Bandwidth	V_{OUT} = 4V_{P-P}, A_V = -1	B	25	-	300	-	MHz
Gain Flatness (Note 3)	To 100MHz	B	25	-	±0.14	-	dB
Gain Flatness	To 50MHz	B	25	-	±0.04	-	dB
Gain Flatness	To 30MHz	B	25	-	±0.01	-	dB
Linear Phase Deviation (Note 3)	DC to 100MHz	B	25	-	0.6	-	Degrees
Differential Gain	NTSC, R_L = 75Ω	B	25	-	0.03	-	%
Differential Phase	NTSC, R_L = 75Ω	B	25	-	0.05	-	Degrees
Minimum Stable Gain		A	Full	1	-	-	V/V
OUTPUT CHARACTERISTICS A_V = +2, Unless Otherwise Specified							
Output Voltage (Note 3)	A_V = -1	A	25	±3.0	±3.3	-	V
		A	Full	±2.5	±3.0	-	V
Output Current	R_L = 50Ω, A_V = -1	A	25, 85	50	60	-	mA
		A	-40	35	50	-	mA
DC Closed Loop Output Impedance (Note 3)		B	25	-	0.07	-	Ω
2nd Harmonic Distortion (Note 3)	30MHz, V_{OUT} = 2V_{P-P}	B	25	-	-56	-	dBc
3rd Harmonic Distortion (Note 3)	30MHz, V_{OUT} = 2V_{P-P}	B	25	-	-80	-	dBc
3rd Order Intercept (Note 3)	100MHz	B	25	20	30	-	dBm
1dB Compression	100MHz	B	25	15	20	-	dBm
TRANSIENT RESPONSE A_V = +2, Unless Otherwise Specified							
Rise Time	V_{OUT} = 2.0V Step	B	25	-	900	-	ps
Overshoot (Note 3)	V_{OUT} = 2.0V Step	B	25	-	10	-	%
Slew Rate	A_V = +1, V_{OUT} = 5V_{P-P}	B	25	-	1400	-	V/µs
Slew Rate	A_V = +2, V_{OUT} = 5V_{P-P}	B	25	1850	2300	-	V/µs
0.1% Settling (Note 3)	V_{OUT} = 2V to 0V	B	25	-	11	-	ns
0.2% Settling (Note 3)	V_{OUT} = 2V to 0V	B	25	-	7	-	ns
Overdrive Recovery Time	2X Overdrive	B	25	-	7.5	10	ns
POWER SUPPLY CHARACTERISTICS							
Supply Voltage Range		B	Full	±4.5	-	±5.5	V
Supply Current (Note 3)		A	25	-	21	26	mA
		A	Full	-	-	33	mA

NOTES:

2. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
3. See Typical Performance Curves for more information.

Application Information

Optimum Feedback Resistor (R_F)

The enclosed plots of inverting and non-inverting frequency response detail the performance of the HFA1100/1120 in various gains. Although the bandwidth dependency on A_{CL} isn't as severe as that of a voltage feedback amplifier, there is an appreciable decrease in bandwidth at higher gains. This decrease can be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and the R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1100, 1120 designs are optimized for a 510Ω R_F, at a gain of +1. Decreasing R_F in a unity gain application decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback causes the same problems due to the feedback impedance decrease at higher frequencies). At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth. The table below lists recommended R_F values for various gains, and the expected bandwidth.

A_{CL}	R_F (Ω)	BW (MHz)
+1	510	850
-1	430	580
+2	360	670
+5	150	520
+10	180	240
+19	270	125

Offset Adjustment

The HFA1120 allows for adjustment of the inverting input bias current to null the output offset voltage. $-I_{BIAS}$ flows through R_F, so any change in bias current forces a corresponding change in output voltage. The amount of adjustment is a function of R_F. With R_F = 510Ω, the typical adjust range is ±100mV. For offset adjustment connect a 10kΩ potentiometer between pins 1 and 5 with the wiper connected to V-.

5V Single Supply Operation

These amplifiers will operate at single supply voltages down to 4.5V. The table below details the amplifier's performance with a single 5V supply. The dramatic supply current reduction at this operating condition (refer also to Figure 23) makes these op amps even better choices for low power 5V systems. Refer to Application Note AN9745 for further information.

PARAMETER	TYP
Input Common Mode Range	1V to 4V
-3dB BW (A_V = +2)	267MHz
Gain Flatness (to 50MHz, A_V = +2)	0.05dB
Output Voltage (A_V = -1)	1.3V to 3.8V
Slew Rate (A_V = +2)	475V/μs
0.1% Settling Time	17ns
Supply Current	5.5mA

Use of Die in Hybrid Applications

These amplifiers are designed with compensation to negate the package parasitics that typically lead to instabilities. As a result, the use of die in hybrid applications results in overcompensated performance due to lower parasitic capacitances. Reducing R_F below the recommended values for packaged units will solve the problem. For A_V = +2 the recommended starting point is 300Ω, while unity gain applications should try 400Ω.

PC Board Layout

The frequency performance of these amplifiers depends a great deal on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value chip (0.1μF) capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance, such as that resulting from an improperly terminated transmission line will degrade the frequency response of the amplifier and may cause oscillations. In most cases, the oscillation can be avoided by placing a resistor in series with the output.

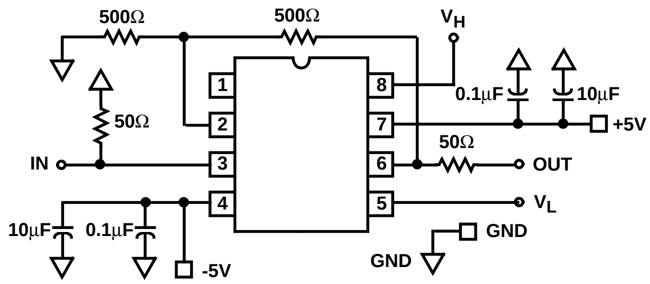
Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to pin 2, and connections to pin 2 should be kept as short as possible.

An example of a good high frequency layout is the Evaluation Board shown below.

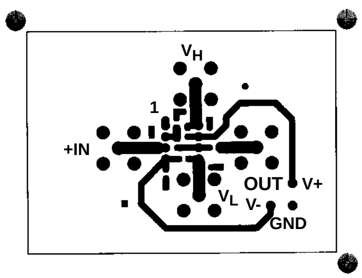
Evaluation Board

An evaluation board is available for the HFA1100 (Part Number HFA11XXEVAL). Please contact your local sales office for information.

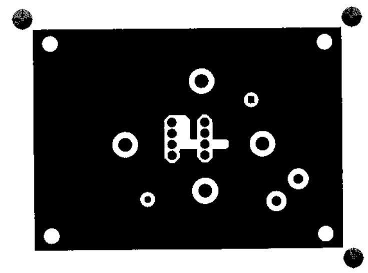
The layout and schematic of the board are shown below:



TOP LAYOUT



BOTTOM LAYOUT



Typical Performance Curves

V_{SUPPLY} = ±5V, R_F = 510Ω, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified

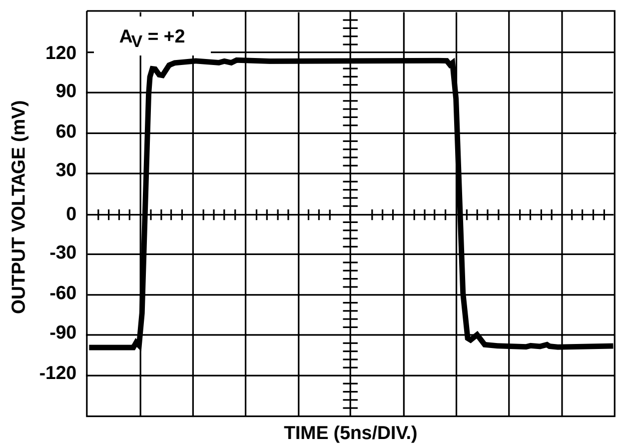


FIGURE 1. SMALL SIGNAL PULSE

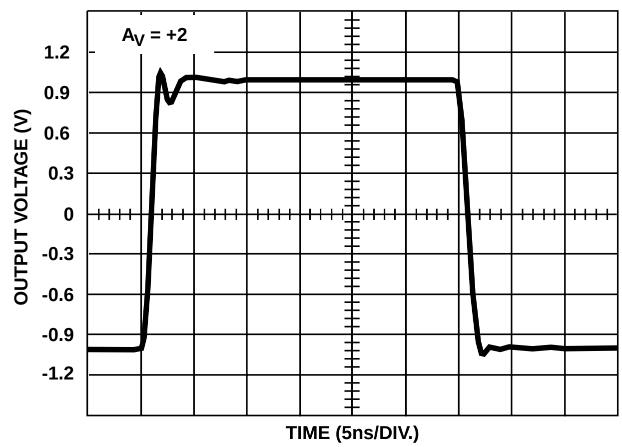


FIGURE 2. LARGE SIGNAL PULSE

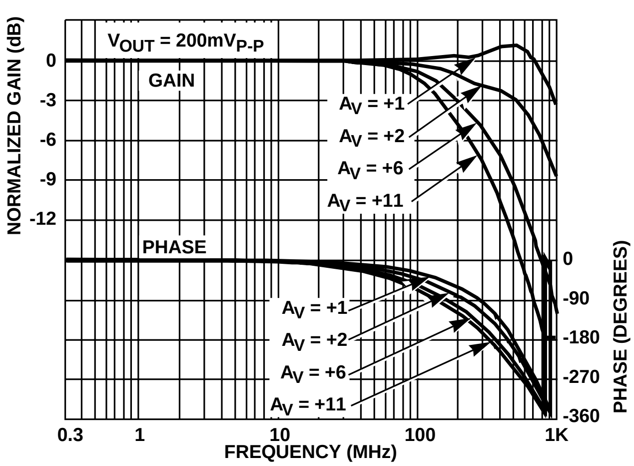


FIGURE 3. NON-INVERTING FREQUENCY RESPONSE

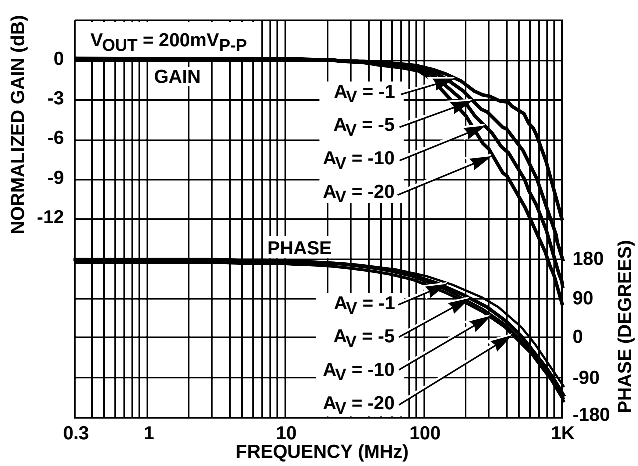


FIGURE 4. INVERTING FREQUENCY RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

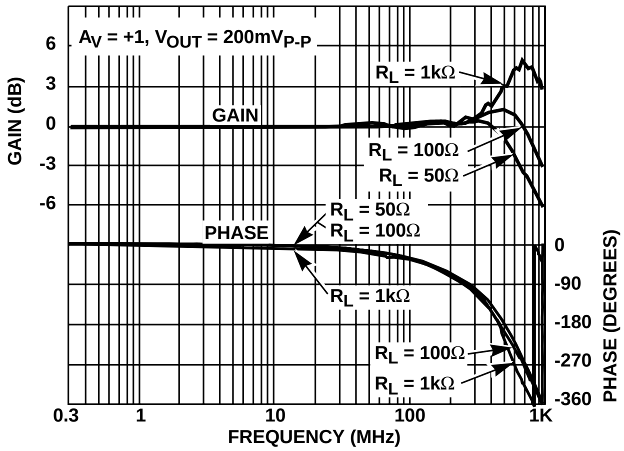


FIGURE 5. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

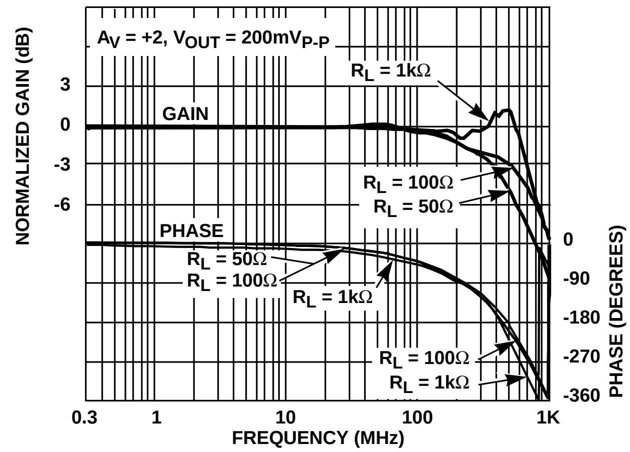


FIGURE 6. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

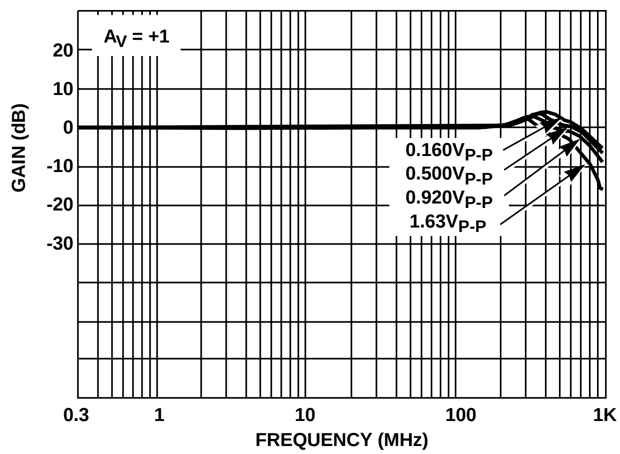


FIGURE 7. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

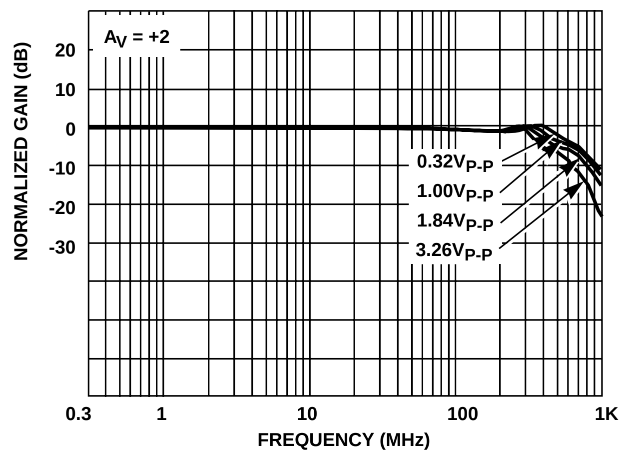


FIGURE 8. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

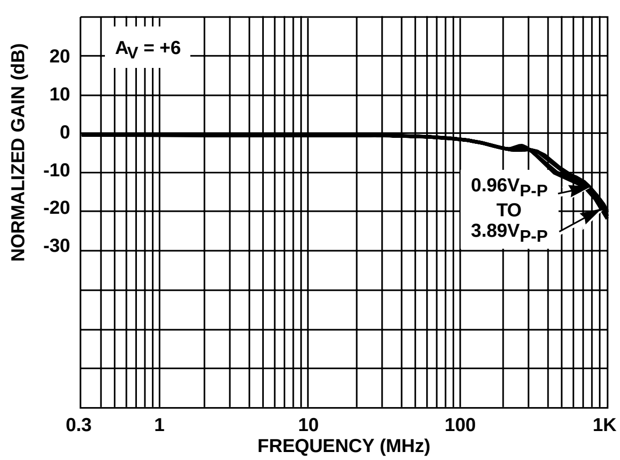


FIGURE 9. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

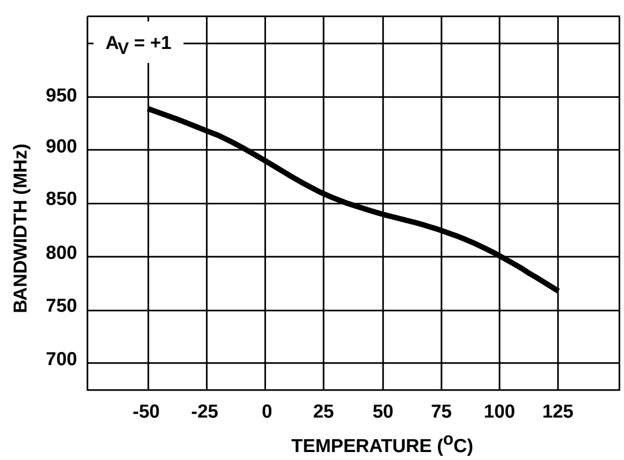


FIGURE 10. -3dB BANDWIDTH vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $R_F = 510\Omega$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

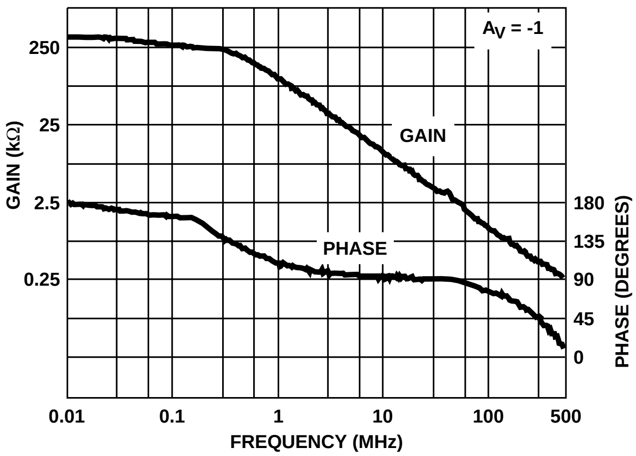


FIGURE 11. OPEN LOOP TRANSIMPEDANCE

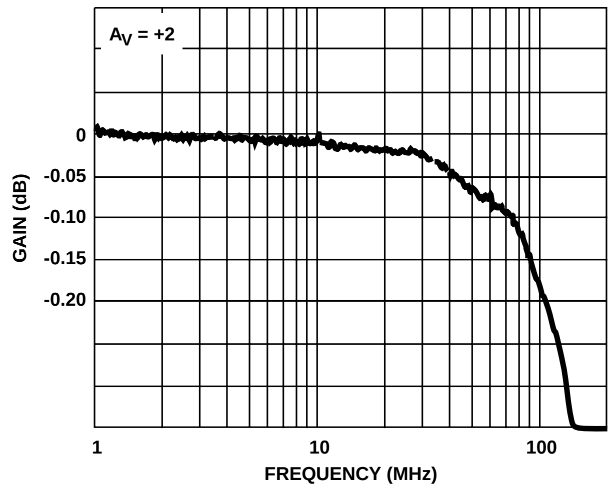


FIGURE 12. GAIN FLATNESS

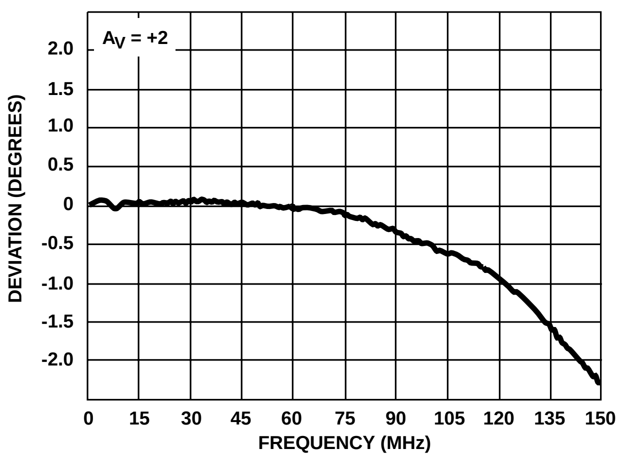


FIGURE 13. DEVIATION FROM LINEAR PHASE

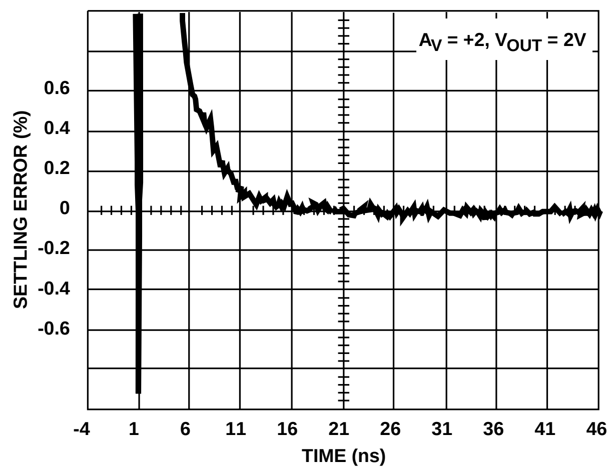


FIGURE 14. SETTLING RESPONSE

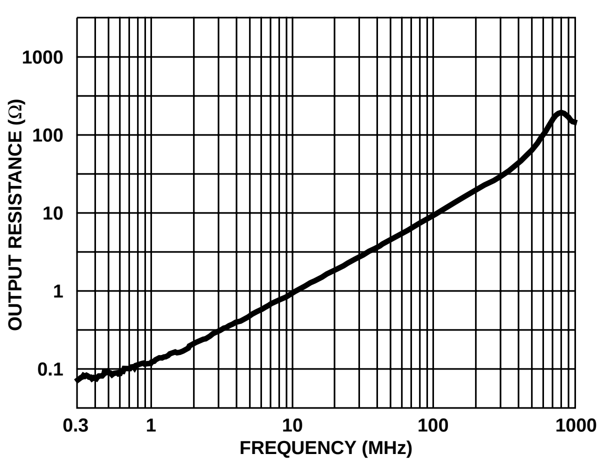


FIGURE 15. CLOSED LOOP OUTPUT RESISTANCE

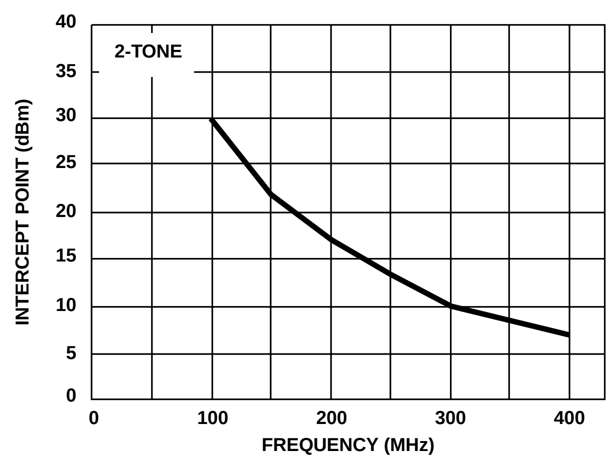


FIGURE 16. 3rd ORDER INTERMODULATION INTERCEPT

Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $R_F = 510\Omega$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

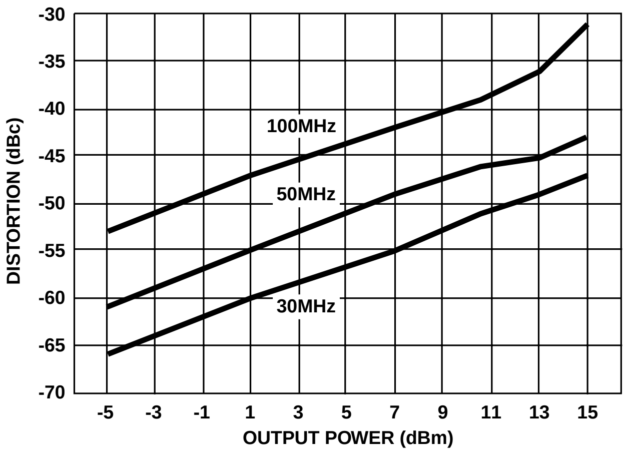


FIGURE 17. 2nd HARMONIC DISTORTION vs P_{OUT}

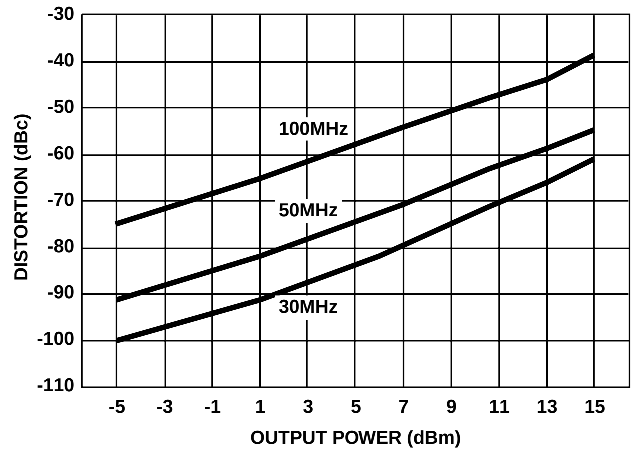


FIGURE 18. 3rd HARMONIC DISTORTION vs P_{OUT}

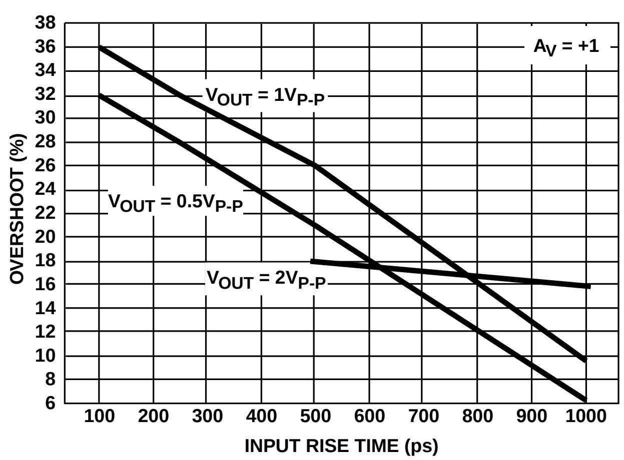


FIGURE 19. OVERSHOOT vs INPUT RISE TIME

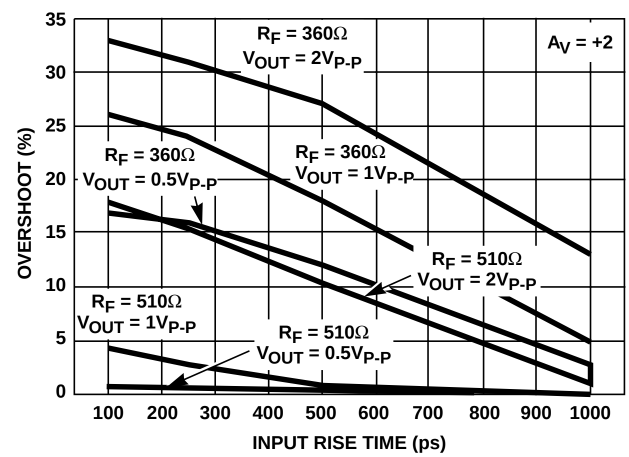


FIGURE 20. OVERSHOOT vs INPUT RISE TIME

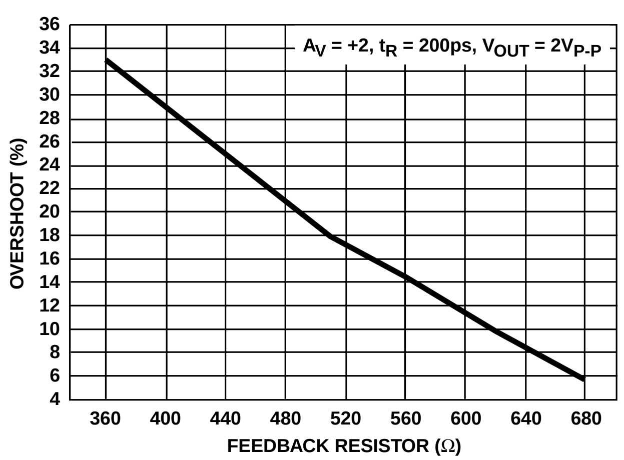


FIGURE 21. OVERSHOOT vs FEEDBACK RESISTOR

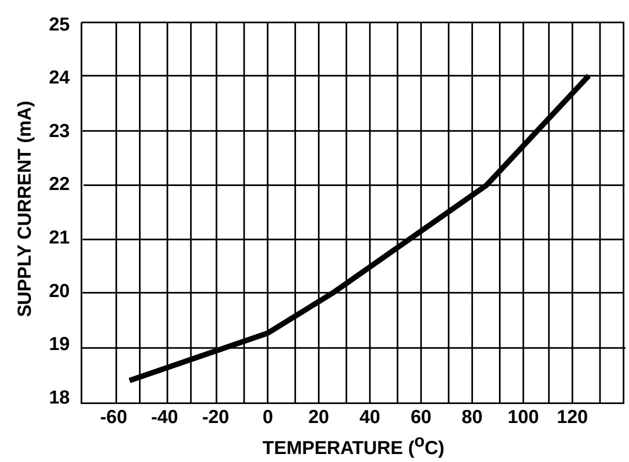


FIGURE 22. SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves V_{SUPPLY} = ±5V, R_F = 510Ω, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

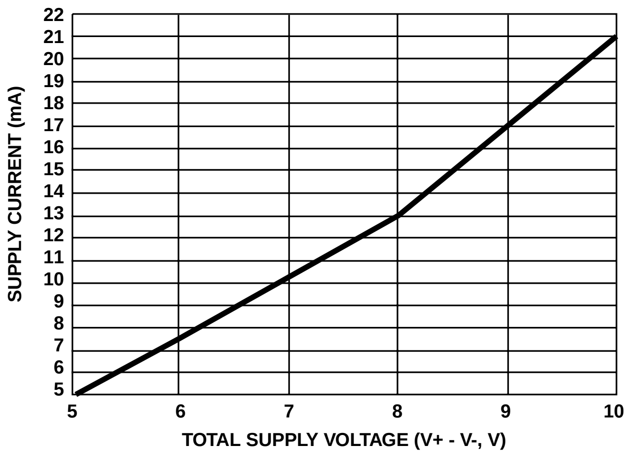


FIGURE 23. SUPPLY CURRENT vs SUPPLY VOLTAGE

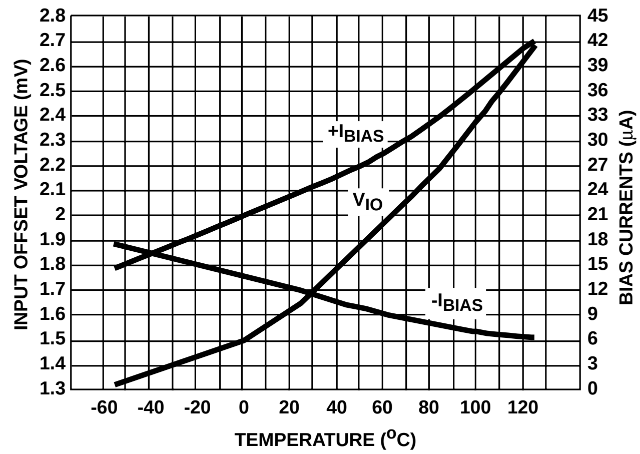


FIGURE 24. V_{IO} AND BIAS CURRENTS vs TEMPERATURE

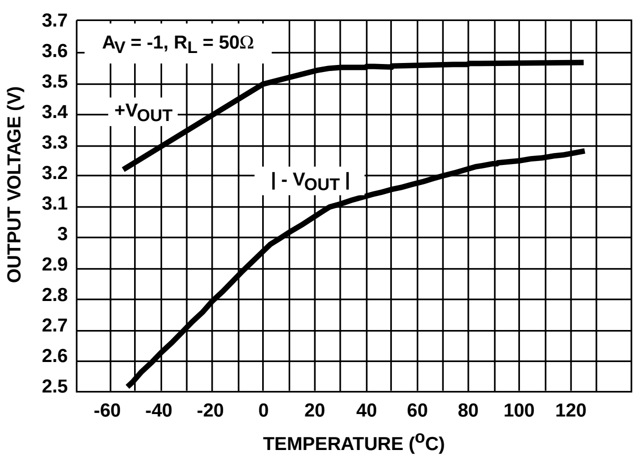


FIGURE 25. OUTPUT VOLTAGE vs TEMPERATURE

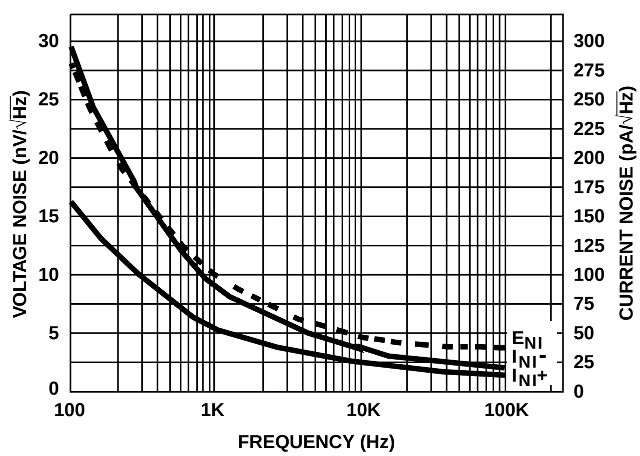


FIGURE 26. INPUT NOISE vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

63 mils x 44 mils x 19 mils
1600µm x 1130µm

METALLIZATION:

Type: Metal 1: AlCu (2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ
Type: Metal 2: AlCu (2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

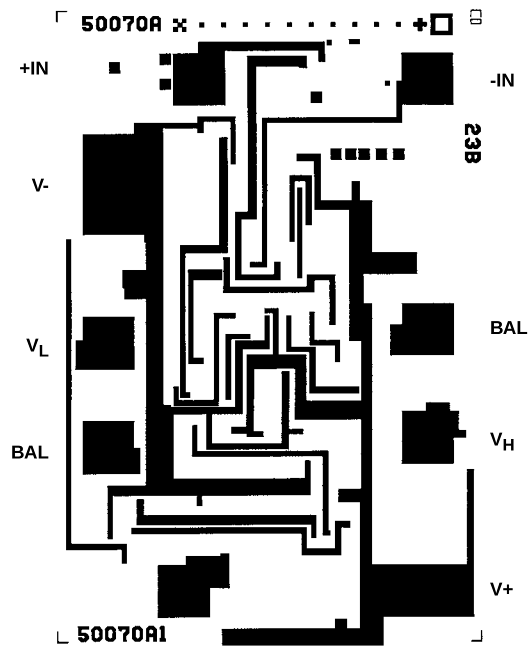
52

SUBSTRATE POTENTIAL (POWERED UP):

Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1100, HFA1120



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.