Data Sheet July 1999 File Number 3574.4

45A, 60V, 0.028 Ohm, N-Channel Power MOSFETs

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA49028.

Ordering Information

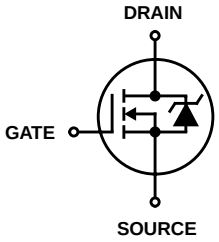
PART NUMBER	PACKAGE	BRAND
RFG45N06	TO-247	RFG45N06
RFP45N06	TO-220AB	RFP45N06
RF1S45N06SM	TO-263AB	F1S45N06

NOTE: When ordering, use the entire part number. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, i.e. RF1S45N06SM9A.

Features

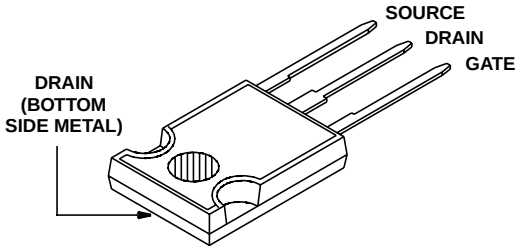
- 45A, 60V
- $r_{DS(ON)} = 0.028\Omega$
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

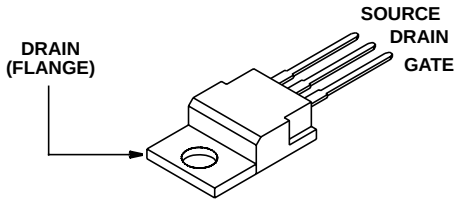


Packaging

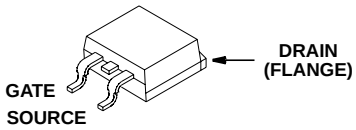
JEDEC STYLE TO-247



JEDEC TO-220AB



JEDEC TO-263AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFG45N06, RFP45N06 RF1S45N06SM	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	60	V
Drain to Gate Voltage (R_G = 20KΩ) (Note 1)	V_{DGR}	60	V
Continuous Drain Current	I_D	45	A
Pulsed Drain Current (Note 3)	I_{DM}	Refer to Peak Current Curve	
Gate to Source Voltage	V_{GS}	±20	V
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation	P_D	131	W
Linear Derating Factor		0.877	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V (Figure 11)		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250µA (Figure 10)		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V		-	-	1	µA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V (125^oC)		-	-	25	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	±100	nA
Drain Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 45A, V_{GS} = 10V (Figure 9)		-	-	0.028	Ω
Turn-On Time	t_{ON}	V_{DD} = 30V, I_D = 45A R_L = 0.667Ω, V_{GS} = +10V R_G = 3.6Ω (Figure 13)		-	-	120	ns
Turn-On Delay Time	$t_{d(ON)}$			-	12	-	ns
Rise Time	t_r			-	74	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	37	-	ns
Fall Time	t_f			-	16	-	ns
Turn-Off Time	t_{OFF}			-	-	80	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0 to 20V	V_{DD} = 48V, I_D = 45A, R_L = 1.07Ω $I_{g(REF)}$ = 1.5mA (Figure 13)	-	125	150	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0 to 10V		-	67	80	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0 to 2V		-	3.7	4.5	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V f = 1MHz (Figure 12)		-	2050	-	pF
Output Capacitance	C_{OSS}			-	600	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	200	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.14	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	80	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 45A	-	-	1.5	V
Diode Reverse Recovery Time	t_{rr}	I_{SD} = 45A, dI_{SD}/dt = 100A/µs	-	-	125	ns

NOTES:

2. Pulse test: pulse width ≤ 300µs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3) and Peak Current Capability Curve (Figure 5).

Typical Performance Curves Unless Otherwise Specified

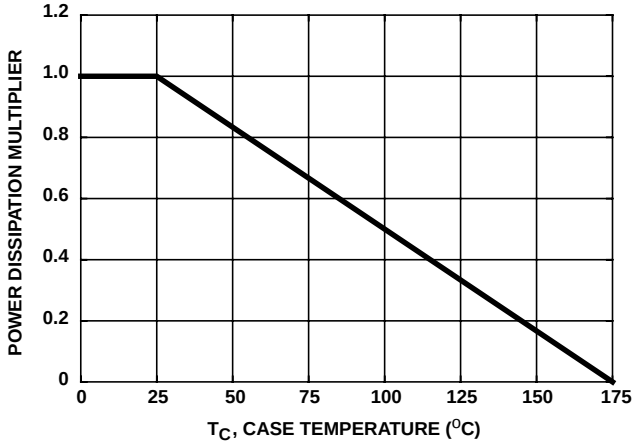


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

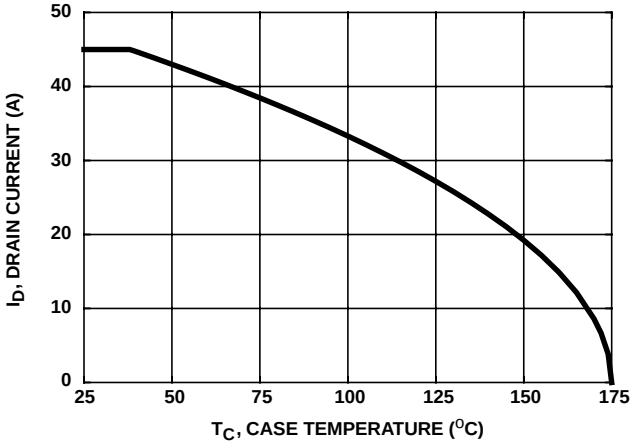


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

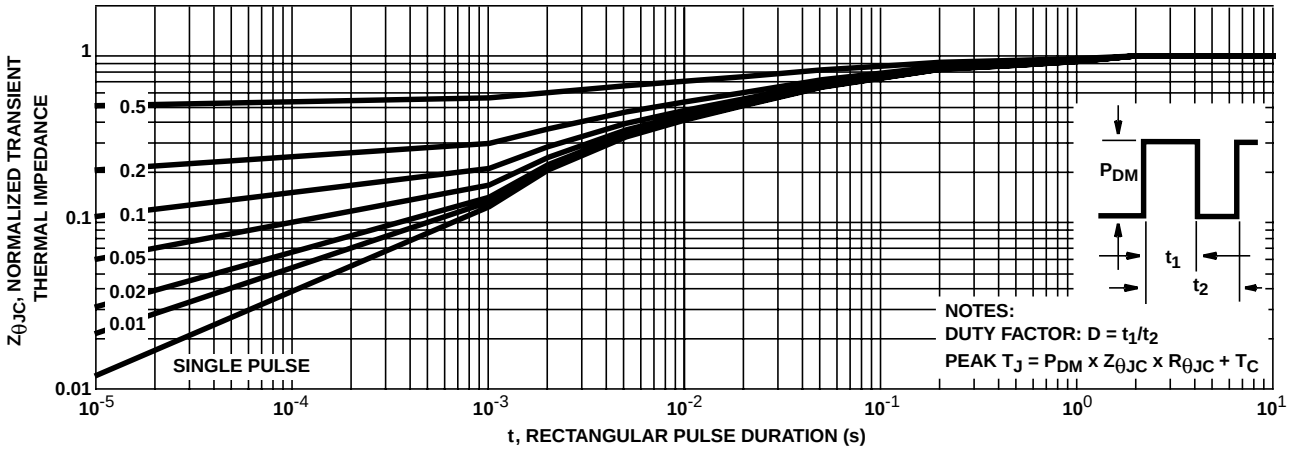


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

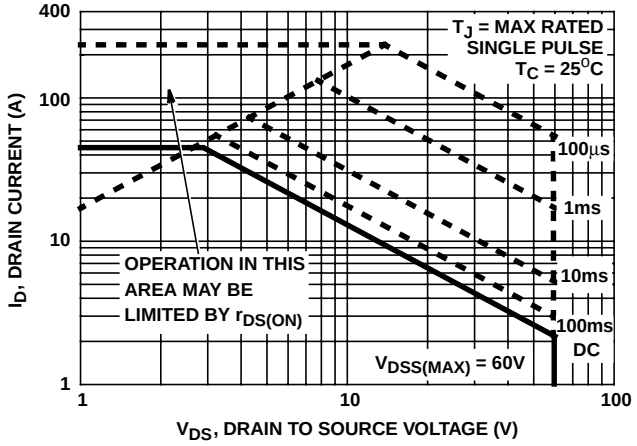


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

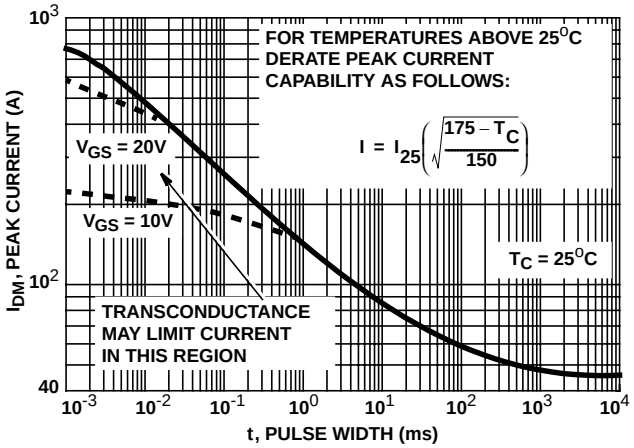
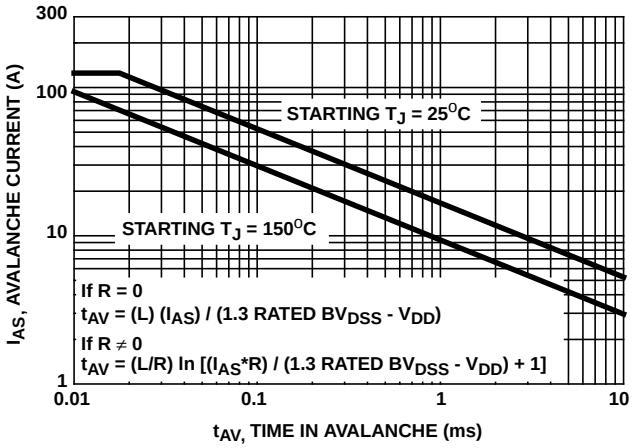


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING

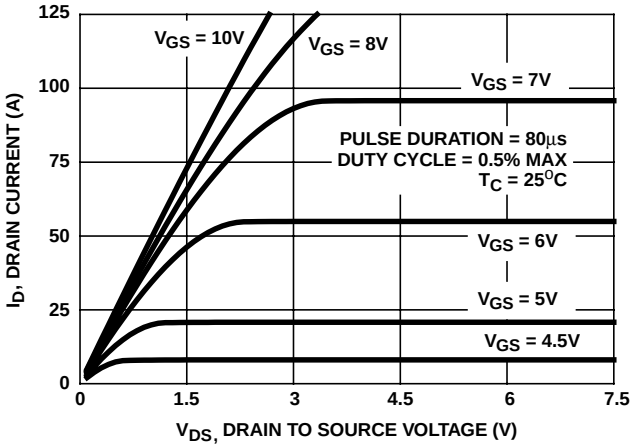


FIGURE 7. SATURATION CHARACTERISTICS

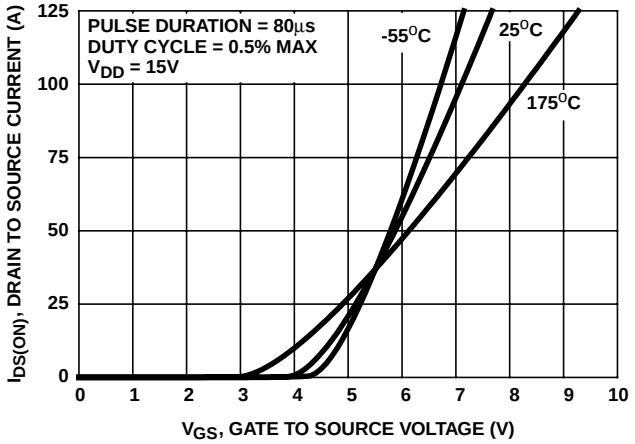


FIGURE 8. TRANSFER CHARACTERISTICS

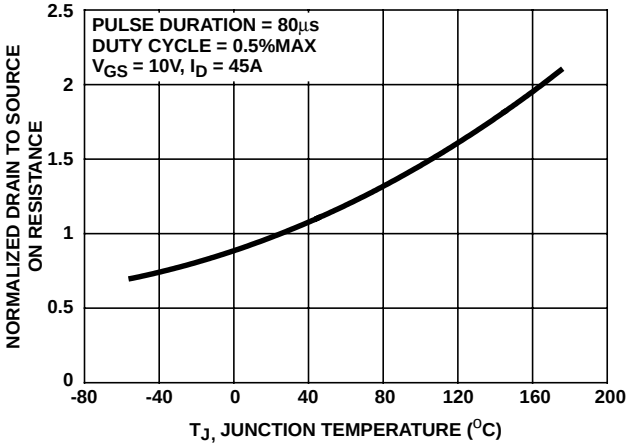


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

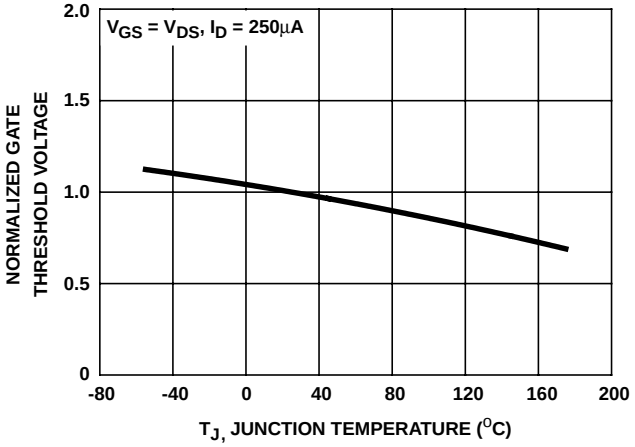


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

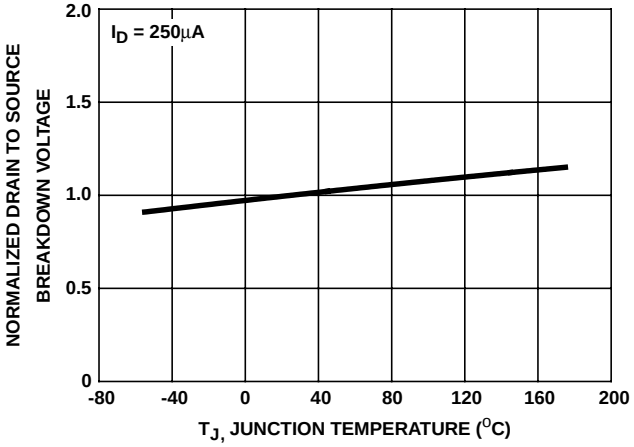


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

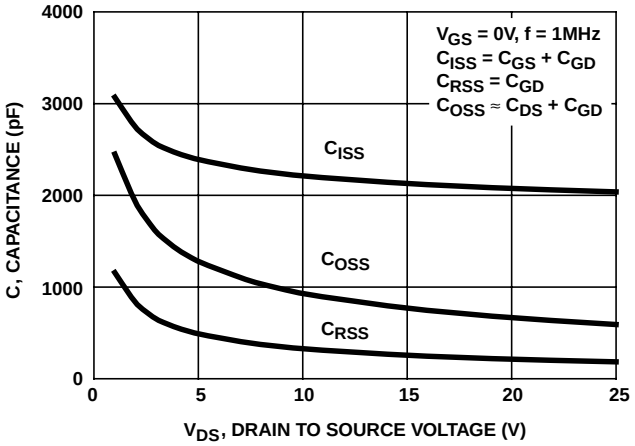
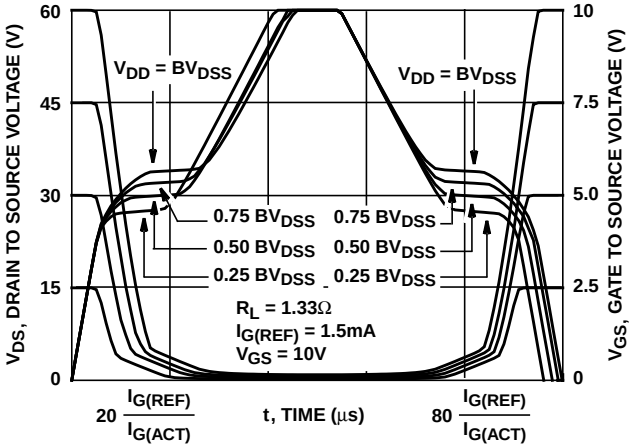


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

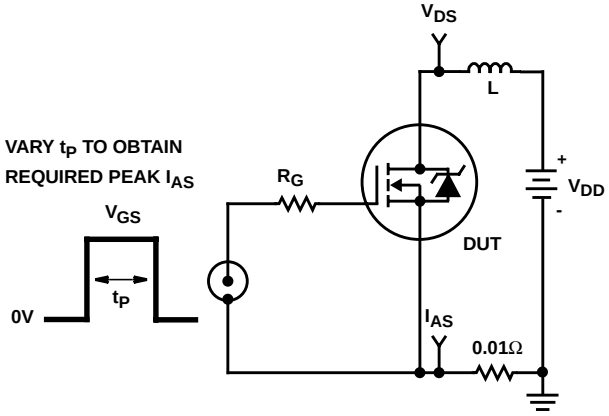


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

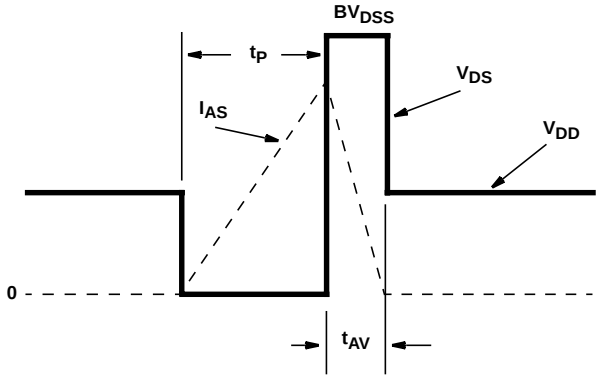


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

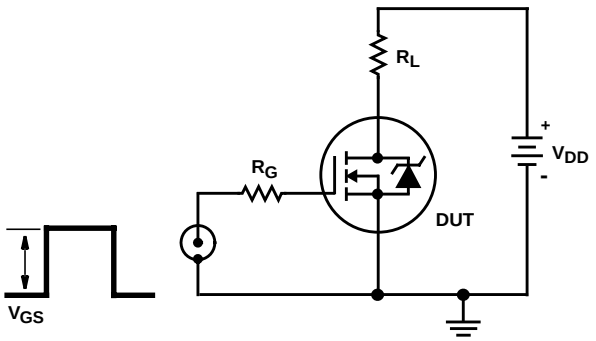


FIGURE 16. SWITCHING TIME TEST CIRCUIT

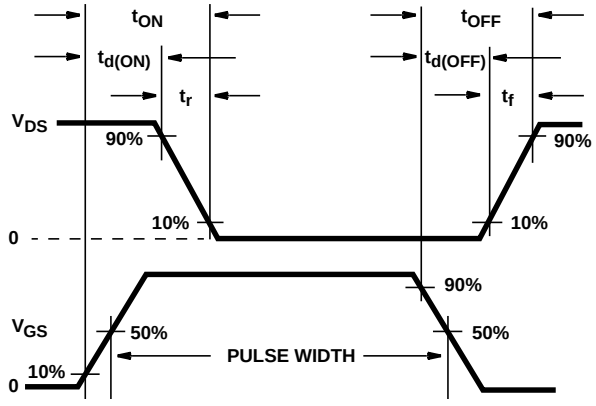


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms

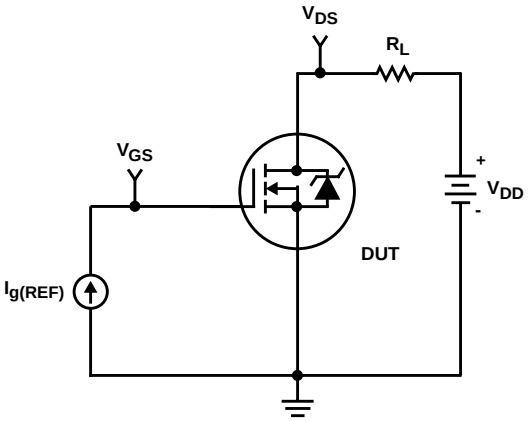


FIGURE 18. GATE CHARGE TEST CIRCUIT

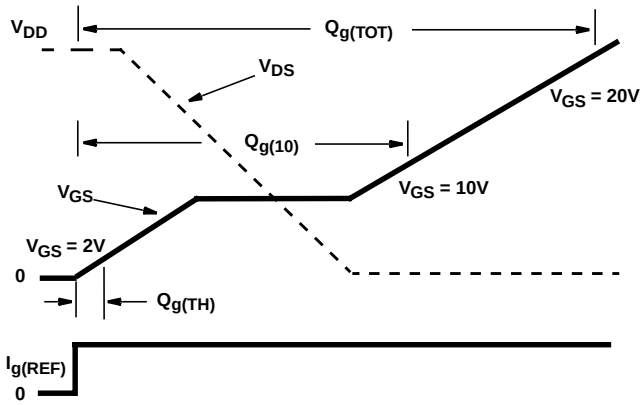
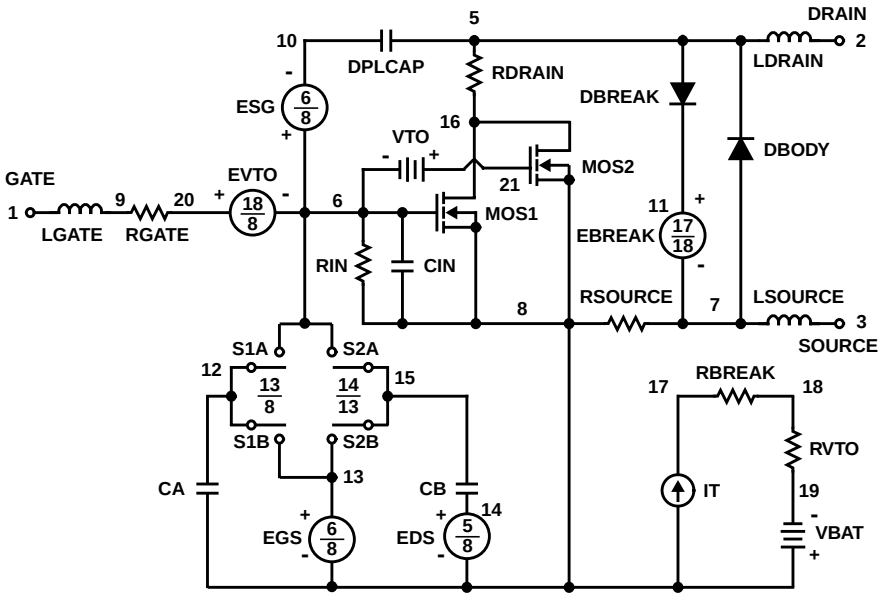


FIGURE 19. GATE CHARGE WAVEFORMS

PSPICE Electrical Model

```
.SUBCKT RFP45N06  2  1  3

 REV 1/18/93

*NOM TEMP = +25OC


CA 12 8 3.49E-9
CB 15 14 3.8E-9
CIN 6 8 2E-9

DBODY 7 5 DBDMOD
DBREAK 5 11DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 66.5
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1E-9
LGATE 1 9 5.65E-9
LSOURCE 3 7 4.13E-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 3.58E-3
RGATE 9 20 0.681
RIN 6 8 1E9
RSOURCE 8 7 RDSMOD 13.6E-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.92

.MODEL DBDMOD D (IS=8.2E-13 RS=7.86E-3 TRS1=2.26E-3 TRS2=2.90E-6 CJO=2.07E-9 TT=5.72E-8)
.MODEL DBKMOD D (RS=1.93E-1 TRS1=5.13E-4 TRS2=-2.15E-5)
.MODEL DPLCAPMOD D (CJO=1.25E-9 IS=1E-30 N=10)
.MODEL MOSMOD NMOS (VTO=3.862 KP=55.57 IS=1E-30 N=10 TOX=1 L=1U W=1U)
.MODEL RBKMOD RES (TC1=1.12E-3 TC2=-5.18E-7)
.MODEL RDSMOD RES (TC1=4.64E-3 TC2=1.58E-5)
.MODEL RVTOMOD RES (TC1=-4.27E-3 TC2=-6.55E-6)
.MODEL S1AMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=-6.5 VOFF=-1.7)
.MODEL S1BMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=-1.7 VOFF=-6.5)
.MODEL S2AMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=-3.0 VOFF=2)
.MODEL S2BMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=2.0 VOFF=-3.0)

.ENDS
```



NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options;** authors, William J. Hepp and C. Frank Wheatley.

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029