Quad, 560MHz, Low Power, Video Operational Amplifier

The HFA1405 is a quad, high speed, low power current feedback amplifier built with Intersil's proprietary complementary bipolar UHF-1 process.

These amplifiers deliver up to 560MHz bandwidth and 1700V/μs slew rate, on only 58mW of quiescent power. They are specifically designed to meet the performance, power, and cost requirements of high volume video applications. The excellent gain flatness and differential gain/phase performance make these amplifiers well suited for component or composite video applications. Video performance is maintained even when driving a back terminated cable (R_L = 150Ω), and degrades only slightly when driving two back terminated cables (R_L = 75Ω). RGB applications will benefit from the high slew rates, and high full power bandwidth.

The HFA1405 is a pin compatible, low power, high performance upgrade for the popular Intersil HA5025, and for the CLC414 and CLC415.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1405IB	-40 to 85	14 Ld SOIC	M14.15
HFA1405IP	-40 to 85	14 Ld PDIP	E14.3
HA5025EVAL	High Speed Op Amp DIP Evaluation Board		

Pinout

**HFA1405
(PDIP, SOIC)**
TOP VIEW
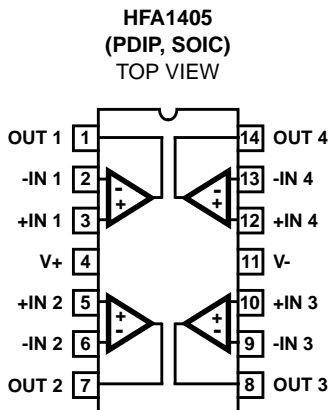
Features

- Low Supply Current . . . . 5.8mA/Op Amp
- High Input Impedance 1MΩ
- Wide -3dB Bandwidth (A_V = +2). 560MHz
- Very Fast Slew Rate 1700V/μs
- Gain Flatness (to 50MHz). . . . . ±0.03dB
- Differential Gain 0.02%
- Differential Phase . . . . 0.03 Degrees
- All Hostile Crosstalk (5MHz). . . . . -60dB
- Pin Compatible Upgrade to HA5025, CLC414, and CLC415

Applications

- Flash A/D Drivers
- Professional Video Processing
- Video Digitizing Boards/Systems
- Multimedia Systems
- RGB Preamps
- Medical Imaging
- Hand Held and Miniaturized RF Equipment
- Battery Powered Communications
- High Speed Oscilloscopes and Analyzers

Absolute Maximum Ratings $T_A = 25^oC$

Voltage Between V+ and V- 11V
DC Input Voltage . . . . V$_{SUPPLY}$
Differential Input Voltage 5V
Output Current (Note 2) . . . . .Short Circuit Protected
30mA Continuous
60mA ≤ 50% Duty Cycle
ESD Rating
   Human Body Model (Per MIL-STD-883 Method 3015.7) . . . 600V

Thermal Information

Thermal Resistance (Typical, Note 1)   θ$_{JA}$ (^{o}C/W)
   SOIC Package   120
   PDIP Package   100
Maximum Junction Temperature (Die) . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . 150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
   (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ$_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

2. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability, however continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.

Electrical Specifications   V$_{SUPPLY}$ = ±5V, A$_V$ = +1, R$_F$ = 510Ω, R$_L$ = 100Ω, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 4) TEST LEVEL	TEMP. (^{o}C)	HFA1405IB (SOIC)			HFA1405IP (PDIP)			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS										
Input Offset Voltage		A	25	-	2	5	-	2	5	mV
		A	Full	-	3	8	-	3	8	mV
Average Input Offset Voltage Drift		B	Full	-	1	10	-	1	10	μV/^{o}C
Input Offset Voltage Common-Mode Rejection Ratio	ΔV$_{CM}$ = ±1.8V	A	25	45	48	-	45	48	-	dB
	ΔV$_{CM}$ = ±1.8V	A	85	43	46	-	43	46	-	dB
	ΔV$_{CM}$ = ±1.2V	A	-40	43	46	-	43	46	-	dB
Input Offset Voltage Power Supply Rejection Ratio	ΔV$_{PS}$ = ±1.8V	A	25	48	52	-	48	52	-	dB
	ΔV$_{PS}$ = ±1.8V	A	85	46	48	-	46	48	-	dB
	ΔV$_{PS}$ = ±1.2V	A	-40	46	48	-	46	48	-	dB
Non-Inverting Input Bias Current		A	25	-	6	15	-	6	15	μA
		A	Full	-	10	25	-	10	25	μA
Non-Inverting Input Bias Current Drift		B	Full	-	5	60	-	5	60	nA/^{o}C
Non-Inverting Input Bias Current Power Supply Sensitivity	ΔV$_{PS}$ = ±1.8V	A	25	-	0.5	1	-	0.5	1	μA/V
	ΔV$_{PS}$ = ±1.8V	A	85	-	0.8	3	-	0.8	3	μA/V
	ΔV$_{PS}$ = ±1.2V	A	-40	-	0.8	3	-	0.8	3	μA/V
Non-Inverting Input Resistance	ΔV$_{CM}$ = ±1.8V	A	25	0.8	1.2	-	0.8	1.2	-	MΩ
	ΔV$_{CM}$ = ±1.8V	A	85	0.5	0.8	-	0.5	0.8	-	MΩ
	ΔV$_{CM}$ = ±1.2V	A	-40	0.5	0.8	-	0.5	0.8	-	MΩ
Inverting Input Bias Current		A	25	-	2	7.5	-	2	7.5	μA
		A	Full	-	5	15	-	5	15	μA
Inverting Input Bias Current Drift		B	Full	-	60	200	-	60	200	nA/^{o}C
Inverting Input Bias Current Common-Mode Sensitivity	ΔV$_{CM}$ = ±1.8V	A	25	-	3	6	-	3	6	μA/V
	ΔV$_{CM}$ = ±1.8V	A	85	-	4	8	-	4	8	μA/V
	ΔV$_{CM}$ = ±1.2V	A	-40	-	4	8	-	4	8	μA/V

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 4) TEST LEVEL	TEMP. (^{o}C)	HFA1405IB (SOIC)			HFA1405IP (PDIP)			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.8V$	A	25	-	2	5	-	2	5	µA/V
	$\Delta V_{PS} = \pm1.8V$	A	85	-	4	8	-	4	8	µA/V
	$\Delta V_{PS} = \pm1.2V$	A	-40	-	4	8	-	4	8	µA/V
Inverting Input Resistance		C	25	-	60	-	-	60	-	Ω
Input Capacitance		B	25	-	1.4	-	-	2.2	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{B-IAS}$ CMS Tests)		A	25, 85	±1.8	±2.4	-	±1.8	±2.4	-	V
		A	-40	±1.2	±1.7	-	±1.2	±1.7	-	V
Input Noise Voltage Density	f = 100kHz	B	25	-	3.5	-	-	3.5	-	nV/√Hz
Non-Inverting Input Noise Current Density	f = 100kHz	B	25	-	2.5	-	-	2.5	-	pA/√Hz
Inverting Input Noise Current Density	f = 100kHz	B	25	-	20	-	-	20	-	pA/√Hz
TRANSFER CHARACTERISTICS										
Open Loop Transimpedance Gain	$A_V = -1$	C	25	-	500	-	-	500	-	kΩ
AC CHARACTERISTICS (Note 3)										
-3dB Bandwidth ($V_{OUT} = 0.2V_{P-P}$, Notes 3, 5)	$A_V = -1$	B	25	-	420	-	-	360	-	MHz
	$A_V = +2$	B	25	-	560	-	-	400	-	MHz
	$A_V = +6$	B	25	-	140	-	-	100	-	MHz
Full Power Bandwidth ($V_{OUT} = 5V_{P-P}$, Notes 3, 5)	$A_V = -1$	B	25	-	260	-	-	260	-	MHz
	$A_V = +2$	B	25	-	165	-	-	165	-	MHz
	$A_V = +6$	B	25	-	140	-	-	100	-	MHz
Gain Flatness ($V_{OUT} = 0.2V_{P-P}$, Notes 3, 5)	$A_V = -1$, To 25MHz	B	25	-	±0.03	-	-	±0.04	-	dB
	$A_V = -1$, To 50MHz	B	25	-	±0.04	-	-	±0.04	-	dB
	$A_V = -1$, To 100MHz	B	25	-	-	-	-	±0.06	-	dB
	$A_V = +2$, To 25MHz	B	25	-	±0.03	-	-	±0.04	-	dB
	$A_V = +2$, To 50MHz	B	25	-	±0.03	-	-	±0.04	-	dB
	$A_V = +2$, To 100MHz	B	25	-	-	-	-	±0.06	-	dB
	$A_V = +6$, To 15MHz	B	25	-	±0.08	-	-	±0.08	-	dB
	$A_V = +6$, To 30MHz	B	25	-	±0.19	-	-	±0.27	-	dB
Minimum Stable Gain		A	Full	-	1	-	-	1	-	V/V
Crosstalk ($A_V = +2$, All Channels Hostile, Note 5)	5MHz	B	25	-	-60	-	-	-55	-	dB
	10MHz	B	25	-	-56	-	-	-52	-	dB
OUTPUT CHARACTERISTICS $A_V = +2$ (Note 3), Unless Otherwise Specified										
Output Voltage Swing (Note 5)	$A_V = -1$, $R_L = 100\Omega$	A	25	±3	±3.4	-	±3	±3.4	-	V
		A	Full	±2.8	±3	-	±2.8	±3	-	V
Output Current (Note 5)	$A_V = -1$, $R_L = 50\Omega$	A	25, 85	50	60	-	50	60	-	mA
		A	-40	28	42	-	28	42	-	mA
Output Short Circuit Current		B	25	-	90	-	-	90	-	mA
Closed Loop Output Impedance		B	25	-	0.2	-	-	0.2	-	Ω
Second Harmonic Distortion ($V_{OUT} = 2V_{P-P}$, Note 5)	10MHz	B	25	-	-51	-	-	-51	-	dBc
	20MHz	B	25	-	-46	-	-	-46	-	dBc

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 4) TEST LEVEL	TEMP. (°C)	HFA1405IB (SOIC)			HFA1405IP (PDIP)			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Third Harmonic Distortion ($V_{OUT} = 2V_{P-P}$, Note 5)	10MHz	B	25	-	-63	-	-	-63	-	dBc
	20MHz	B	25	-	-56	-	-	-56	-	dBc
TRANSIENT CHARACTERISTICS $A_V = +2$ (Note 3), Unless Otherwise Specified										
Rise and Fall Times ($V_{OUT} = 0.5V_{P-P}$, Note 3)	$A_V = +2$	B	25	-	0.8	-	-	0.9	-	ns
	$A_V = +6$	B	25	-	2.9	-	-	4	-	ns
Overshoot ($V_{OUT} = 0.5V_{P-P}$, V_{IN} $t_{RISE} = 1ns$, Notes 3, 6)	$A_V = -1$, +OS	B	25	-	7	-	-	3	-	%
	$A_V = -1$, -OS	B	25	-	8	-	-	13	-	%
	$A_V = +2$, +OS	B	25	-	5	-	-	7	-	%
	$A_V = +2$, -OS	B	25	-	10	-	-	11	-	%
	$A_V = +6$, +OS	B	25	-	2	-	-	2	-	%
	$A_V = +6$, -OS	B	25	-	2	-	-	2	-	%
Slew Rate ($V_{OUT} = 5V_{P-P}$, Notes 3, 5)	$A_V = -1$, +SR	B	25	-	2500	-	-	2500	-	V/μs
	$A_V = -1$, -SR	B	25	-	1900	-	-	1900	-	V/μs
	$A_V = +2$, +SR	B	25	-	1700	-	-	1600	-	V/μs
	$A_V = +2$, -SR	B	25	-	1700	-	-	1400	-	V/μs
	$A_V = +6$, +SR	B	25	-	1500	-	-	1000	-	V/μs
	$A_V = +6$, -SR	B	25	-	1100	-	-	1000	-	V/μs
Settling Time ($V_{OUT} = +2V$ to 0V Step, Note 5)	To 0.1%	B	25	-	23	-	-	23	-	ns
	To 0.05%	B	25	-	30	-	-	30	-	ns
	To 0.025%	B	25	-	37	-	-	40	-	ns
Overdrive Recovery Time	$V_{IN} = \pm2V$	B	25	-	8.5	-	-	8.5	-	ns
VIDEO CHARACTERISTICS $A_V = +2$ (Note 3), Unless Otherwise Specified										
Differential Gain (f = 3.58MHz)	$R_L = 150\Omega$	B	25	-	0.02	-	-	0.03	-	%
	$R_L = 75\Omega$	B	25	-	0.03	-	-	0.06	-	%
Differential Phase (f = 3.58MHz)	$R_L = 150\Omega$	B	25	-	0.03	-	-	0.03	-	Degrees
	$R_L = 75\Omega$	B	25	-	0.06	-	-	0.06	-	Degrees
POWER SUPPLY CHARACTERISTICS										
Power Supply Range		C	25	±4.5	-	±5.5	±4.5	-	±5.5	V
Power Supply Current (Note 5)		A	25	-	5.8	6.1	-	5.8	6.1	mA/Op Amp
		A	Full	-	5.9	6.3	-	5.9	6.3	mA/Op Amp

NOTES:

3. The optimum feedback resistor depends on closed loop gain and package type. The following resistors were used for the PDIP/SOIC characterization: $A_V = -1$, $R_F = 310\Omega/360\Omega$; $A_V = +2$, $R_F = 402\Omega/510\Omega$; $A_V = +6$, $R_F = 500\Omega/500\Omega$. See the Application Information section for more information.

4. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.

5. See Typical Performance Curves for more information.

6. Undershoot dominates for output signal swings below GND (e.g., $2V_{P-P}$), yielding a higher overshoot limit compared to the $V_{OUT} = 0V$ to 2V condition. See the "Application Information" section for details.

Application Information

Performance Differences Between PDIP and SOIC

The amplifiers comprising the HFA1405 are high frequency current feedback amplifiers. As such, they are sensitive to feedback capacitance which destabilizes the op amp and causes overshoot and peaking. Unfortunately, the standard quad op amp pinout places the amplifier's output next to its inverting input, thus making the package capacitance an unavoidable parasitic feedback capacitor. The larger parasitic capacitance of the PDIP requires an inherently more stable amplifier, which yields a PDIP device with lower performance than the SOIC device - see Electrical Specification tables for details.

Because of these performance differences, designers should evaluate and breadboard with the same package style to be used in production.

Note that the "Typical Performance Curves" section has separate pulse and frequency response graphs for each package type. Graphs not labeled with a specific package type are applicable to both packages.

Optimum Feedback Resistor

Although a current feedback amplifier's bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1405 design is optimized for $R_F = 402\Omega/510\Omega$ (PDIP/SOIC) at a gain of +2. Decreasing R_F decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback causes the same problems due to the feedback impedance decrease at higher frequencies). However, at higher gains the amplifier is more stable so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth. For good channel-to-channel gain matching, it is recommended that all resistors (termination as well as gain setting) be ±1% tolerance or better.

OPTIMUM FEEDBACK RESISTOR

GAIN (A_{CL})	R_F (Ω) PDIP/SOIC	BANDWIDTH (MHz) PDIP/SOIC
-1	310/360	360/420
+2	402/510	400/560
+6	500/500 (Note)	100/140

NOTE: $R_F = 500\Omega$ is not the optimum value. It was chosen to match the R_F of the CLC414 and CLC415, for performance comparison purposes. Performance at $A_V = +6$ may be increased by reducing R_F below 500Ω.

Non-inverting Input Source Impedance

For best operation, the DC source impedance seen by the non-inverting input should be $\geq 50\Omega$. This is especially important in inverting gain configurations where the non-inverting input would normally be connected directly to GND.

Pulse Undershoot

The HFA1405 utilizes a quasi-complementary output stage to achieve high output current while minimizing quiescent supply current. In this approach, a composite device replaces the traditional PNP pulldown transistor. The composite device switches modes after crossing 0V, resulting in added distortion for signals swinging below ground, and an increased undershoot on the negative portion of the output waveform (see Figure 6 and Figure 9). This undershoot isn't present for small bipolar signals, or large positive signals (see Figure 5 and Figure 8).

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance, parasitic or planned, connected to the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and eventual instability. To reduce this capacitance the designer should remove the ground plane under traces connected to -IN, and keep connections to -IN as short as possible.

An example of a good high frequency layout is the Evaluation Board shown in Figure 3.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 560MHz. By decreasing R_S as C_L increases (as illustrated in the curve), the maximum bandwidth is obtained without sacrificing stability. In spite of this, bandwidth still decreases as the load capacitance increases.

FIGURE 2. EVALUATION BOARD SCHEMATIC

FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

TOP LAYOUT

Evaluation Board

The performance of the HFA1405 (PDIP) may be evaluated using the HA5025 Evaluation Board.

The schematic for amplifier 1 and the board layout are shown in Figure 2 and Figure 3. Resistors R_F, R_G, and R_S may require a change to values applicable to the HFA1405.

To order evaluation boards (part number HA5025EVAL), please contact your local sales office.

BOTTOM LAYOUT

FIGURE 3. EVALUATION BOARD LAYOUT

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, R_F = Value From the Optimum Feedback Resistor Table, $R_L = 100\Omega$, Unless Otherwise Specified
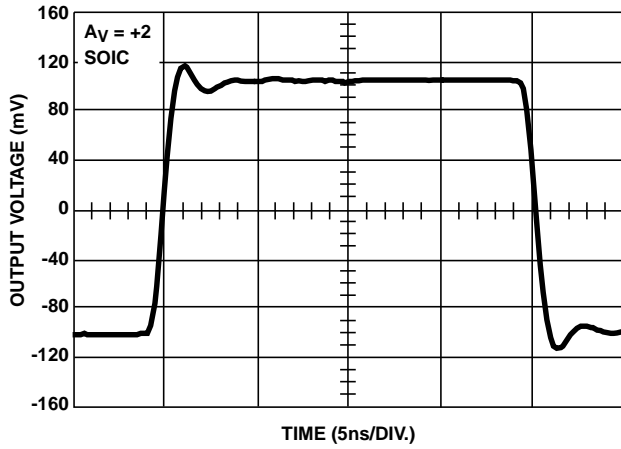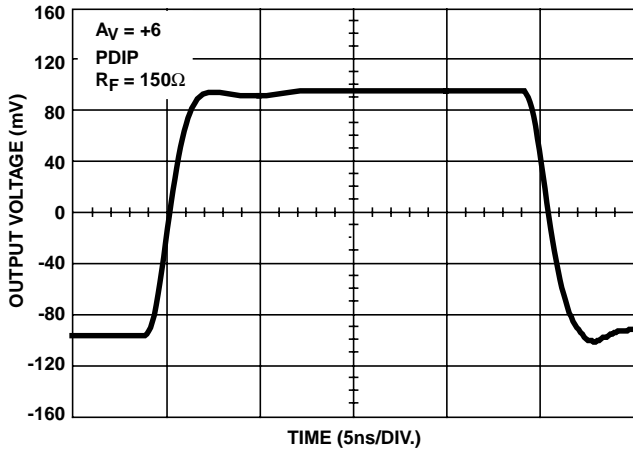
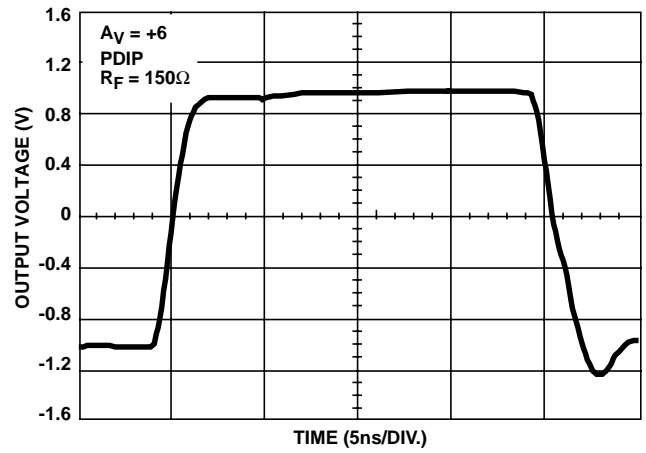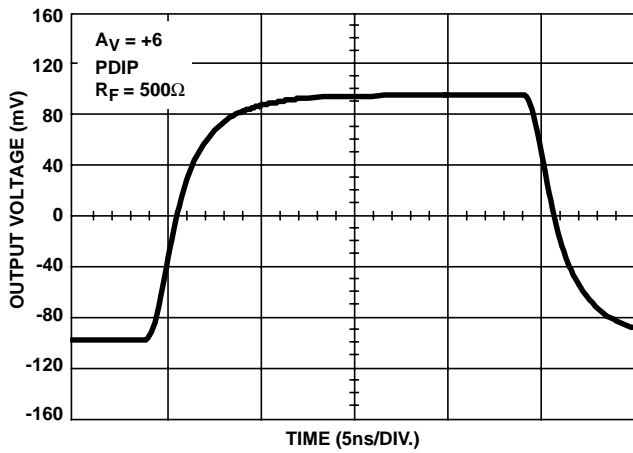FIGURE 4. SMALL SIGNAL PULSE RESPONSE
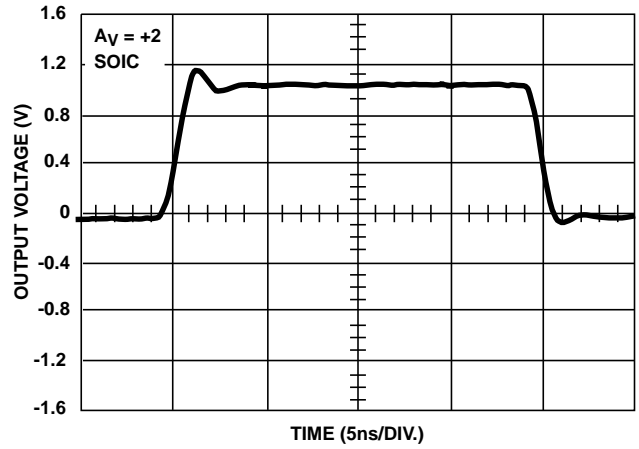
FIGURE 5. LARGE SIGNAL PULSE RESPONSE
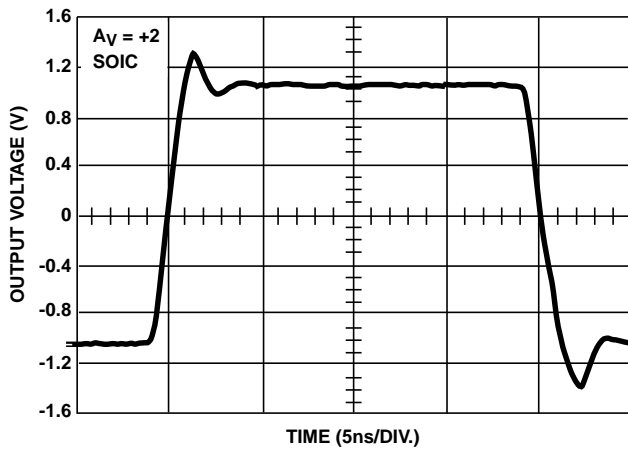
FIGURE 6. LARGE SIGNAL PULSE RESPONSE
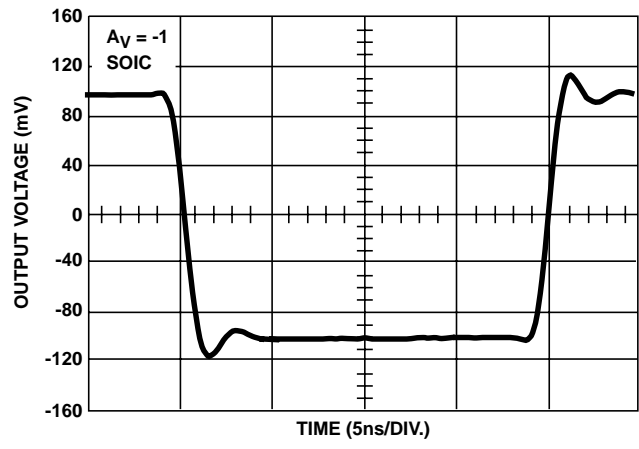
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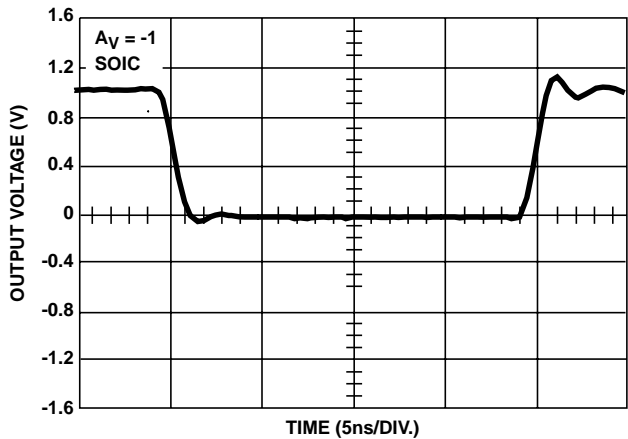
FIGURE 8. LARGE SIGNAL PULSE RESPONSE
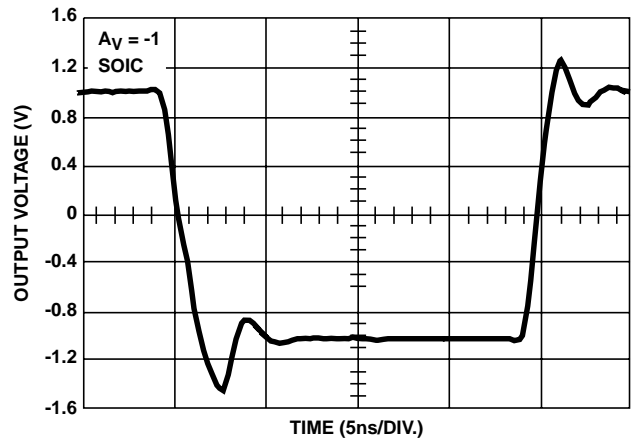
FIGURE 9. LARGE SIGNAL PULSE RESPONSE
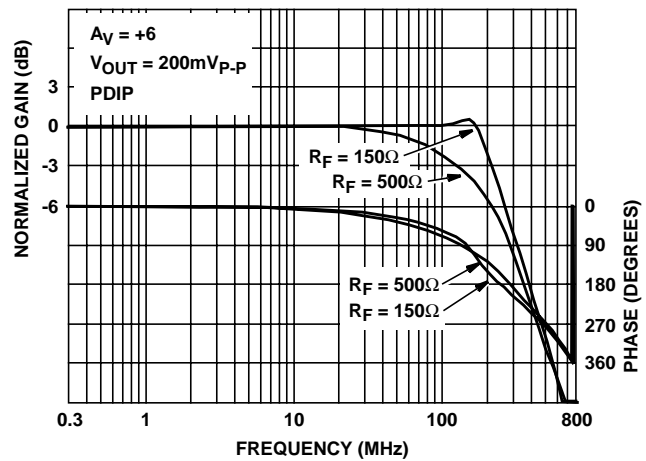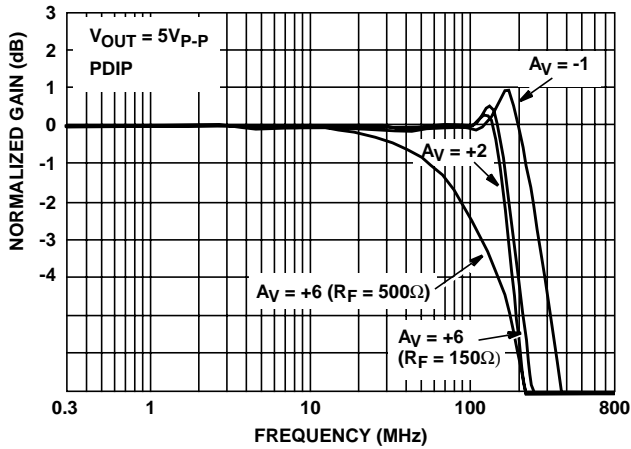
Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, R_F = Value From the Optimum Feedback Resistor Table, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**
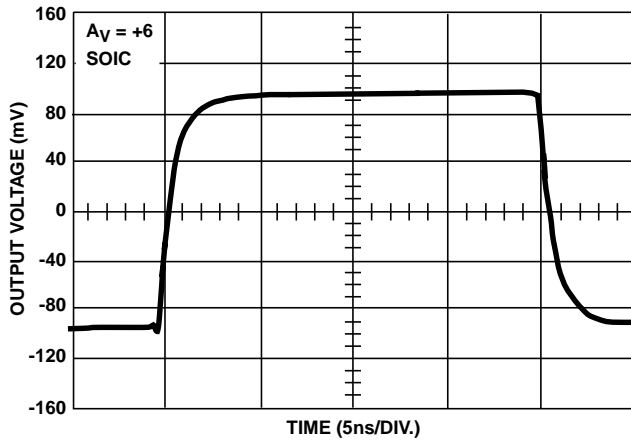
FIGURE 10. SMALL SIGNAL PULSE RESPONSE
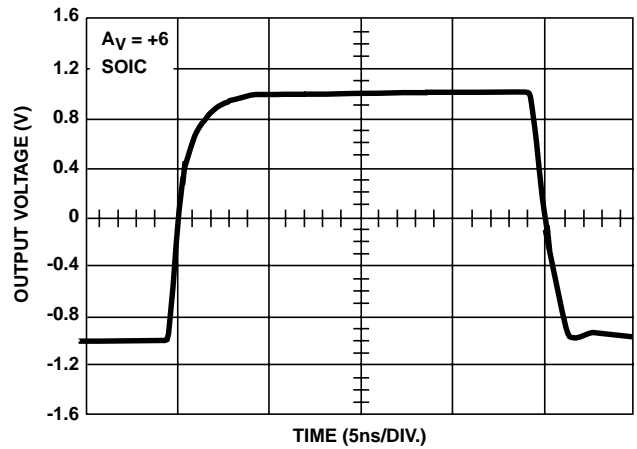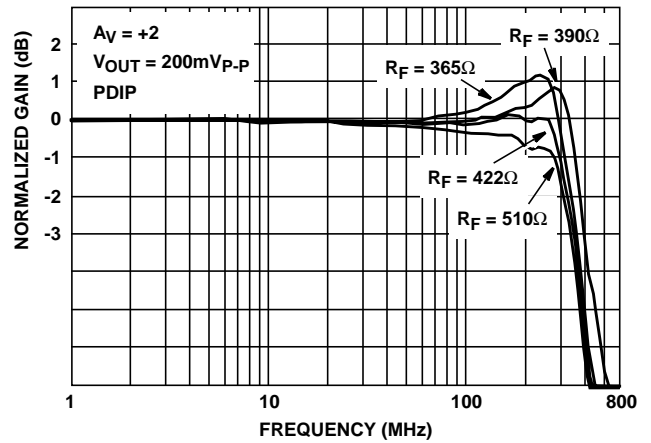

FIGURE 11. LARGE SIGNAL PULSE RESPONSE
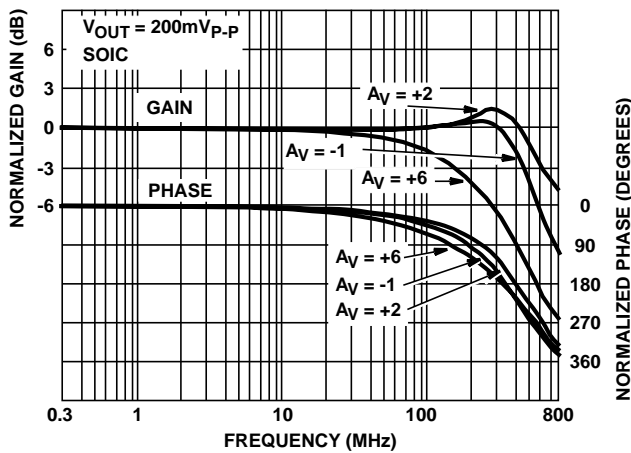
FIGURE 12. FREQUENCY RESPONSE
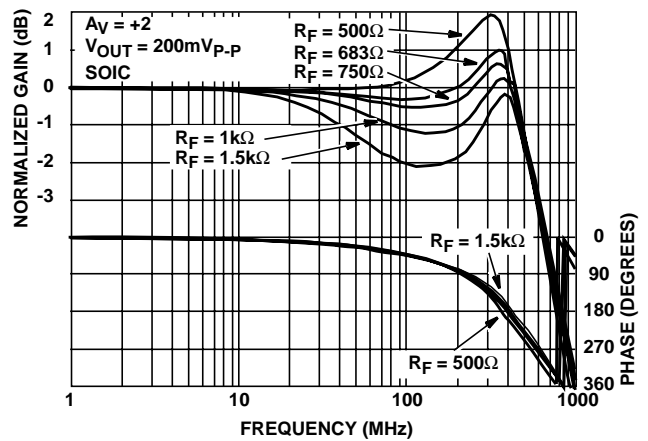
FIGURE 13. FREQUENCY RESPONSE vs FEEDBACK RESISTOR
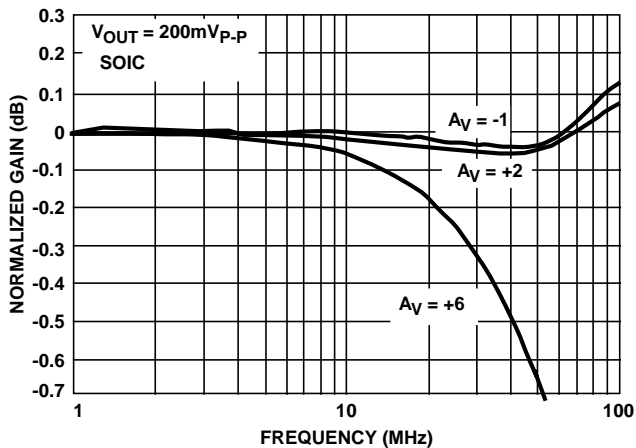
FIGURE 14. GAIN FLATNESS
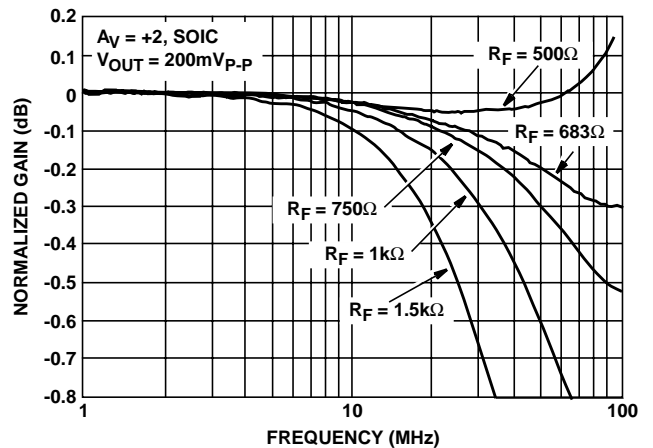
FIGURE 15. GAIN FLATNESS vs FEEDBACK RESISTOR

Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $T_A = 25^oC$, R_F = Value From the Optimum Feedback Resistor Table, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**
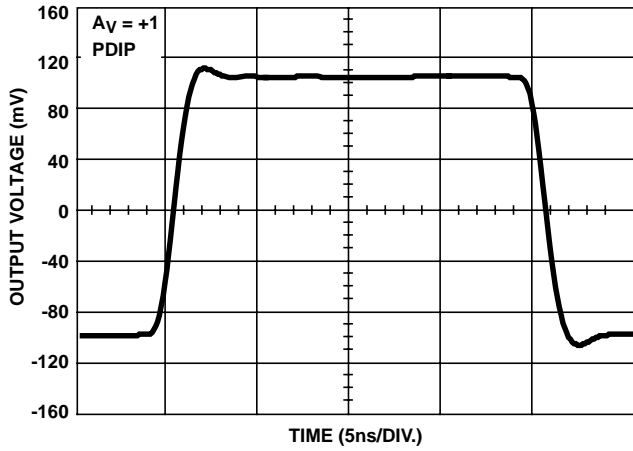
FIGURE 16. SMALL SIGNAL PULSE RESPONSE
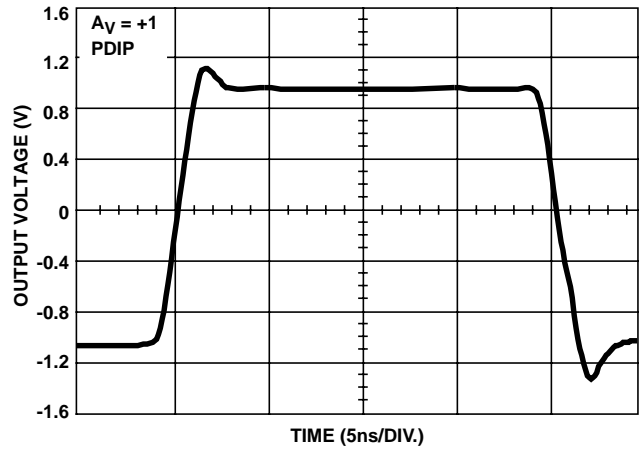
FIGURE 17. LARGE SIGNAL PULSE RESPONSE
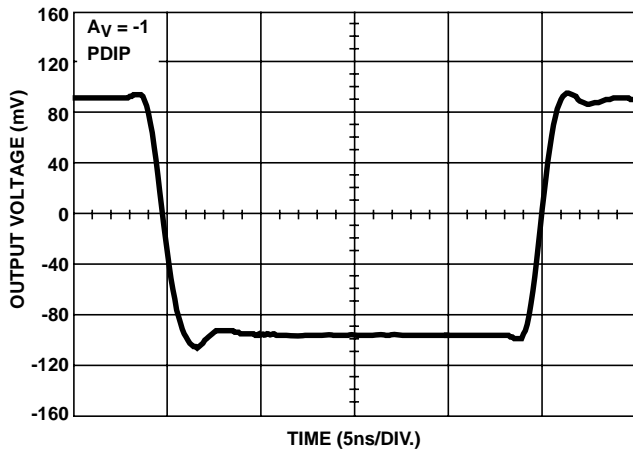
FIGURE 18. SMALL SIGNAL PULSE RESPONSE
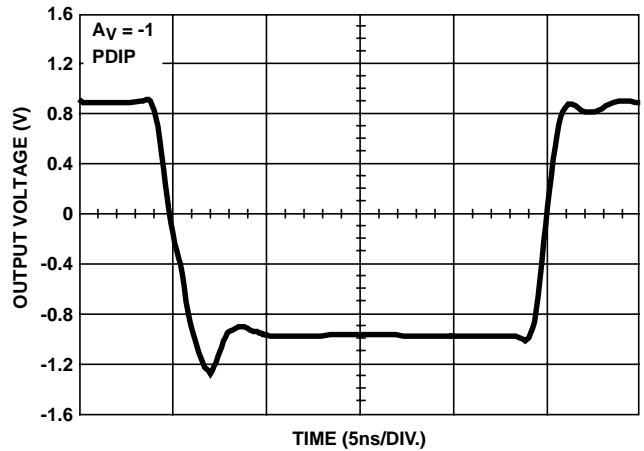
FIGURE 19. LARGE SIGNAL PULSE RESPONSE
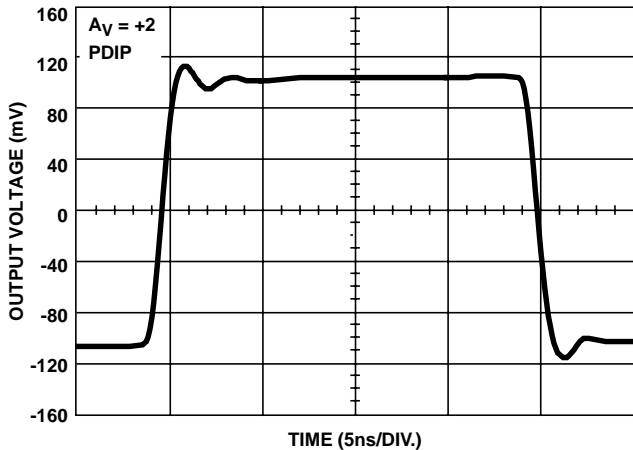
FIGURE 20. SMALL SIGNAL PULSE RESPONSE
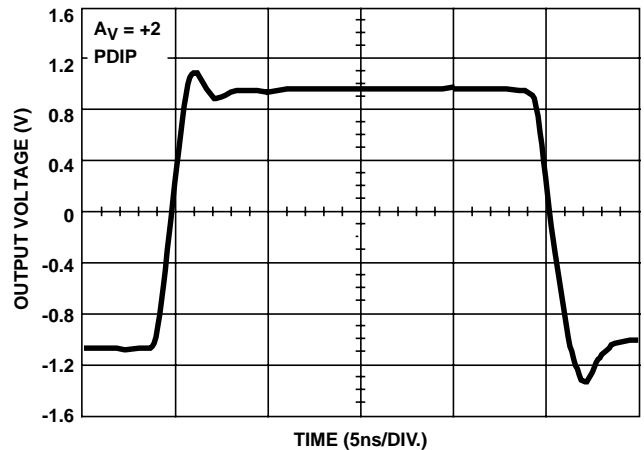
FIGURE 21. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves
V_{SUPPLY} = ±5V, T_A = 25°C, R_F = Value From the Optimum Feedback Resistor Table, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

FIGURE 22. SMALL SIGNAL PULSE RESPONSE

FIGURE 23. LARGE SIGNAL PULSE RESPONSE

FIGURE 24. SMALL SIGNAL PULSE RESPONSE
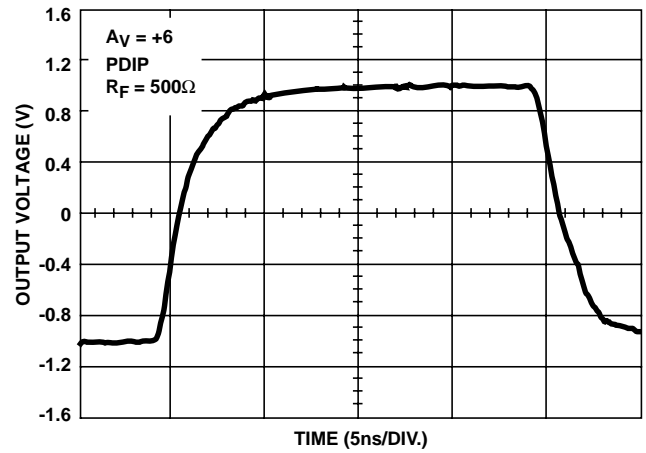
FIGURE 25. LARGE SIGNAL PULSE RESPONSE
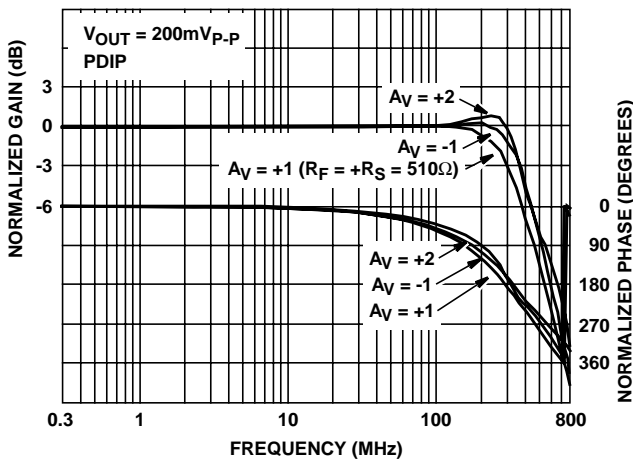
FIGURE 26. FREQUENCY RESPONSE

FIGURE 27. FREQUENCY RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, R_F = Value From the Optimum Feedback Resistor Table, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

FIGURE 28. FULL POWER BANDWIDTH

FIGURE 29. FREQUENCY RESPONSE vs FEEDBACK RESISTOR
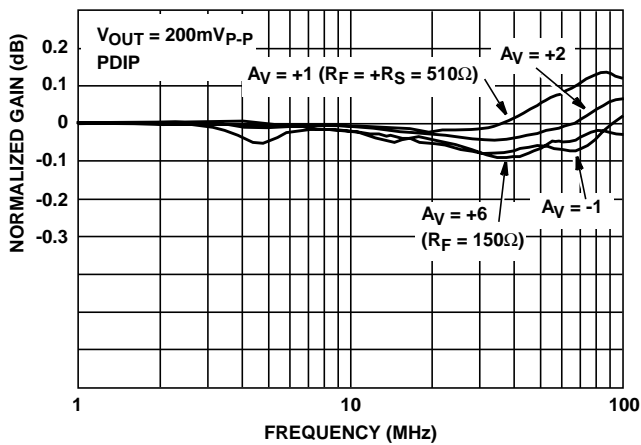
FIGURE 30. GAIN FLATNESS
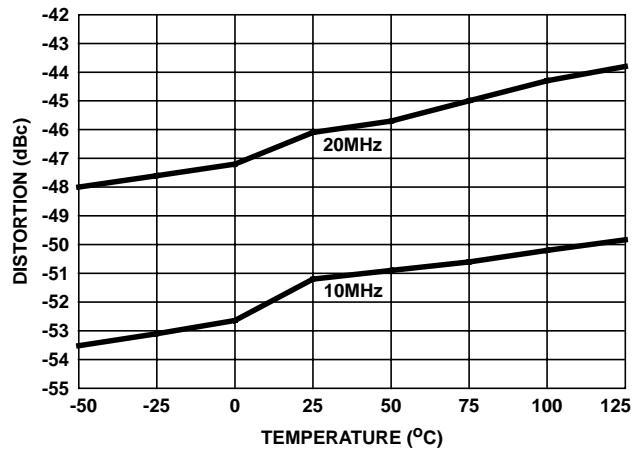
FIGURE 31. 2nd HARMONIC DISTORTION vs TEMPERATURE
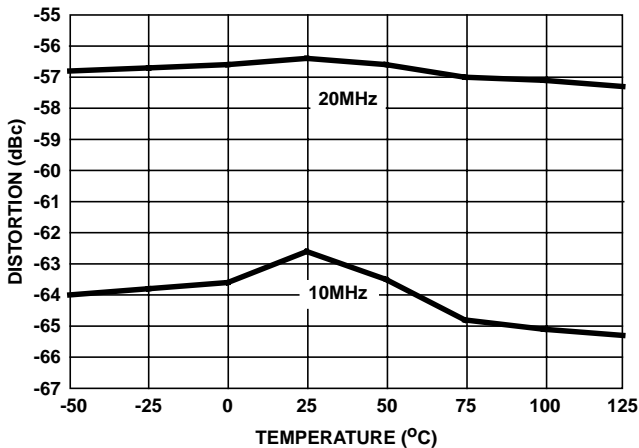
FIGURE 32. 3rd HARMONIC DISTORTION vs TEMPERATURE
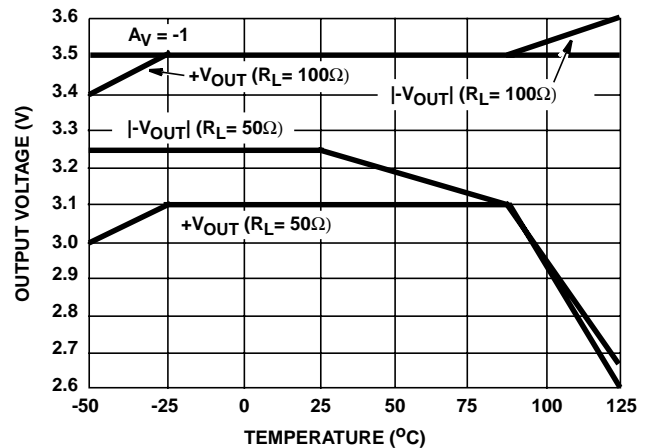
FIGURE 33. OUTPUT VOLTAGE vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, R_F = Value From the Optimum Feedback Resistor Table, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**
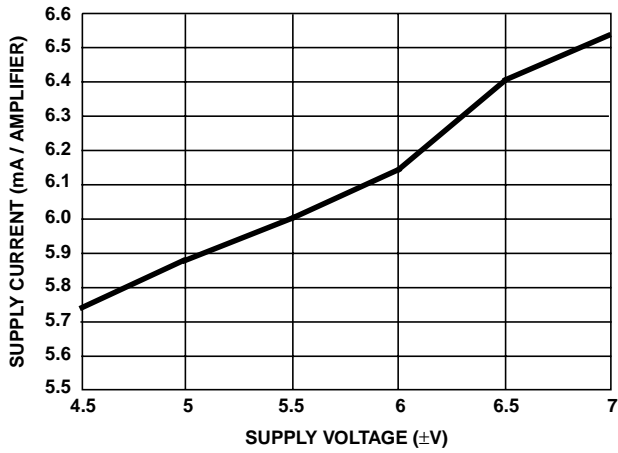
FIGURE 34. SUPPLY CURRENT vs SUPPLY VOLTAGE
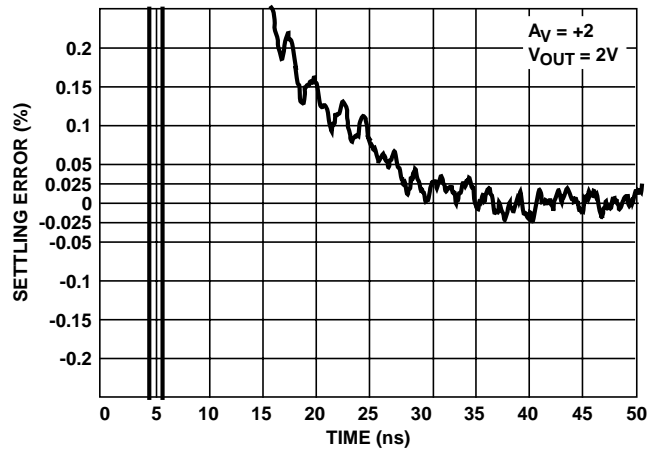
FIGURE 35. SETTLING RESPONSE
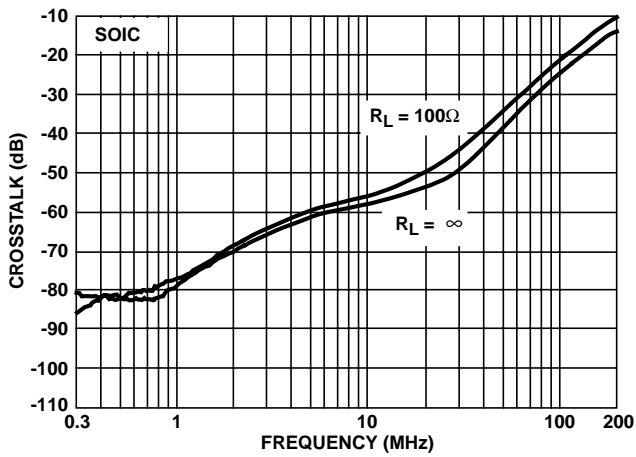
FIGURE 36. ALL HOSTILE CROSSTALK
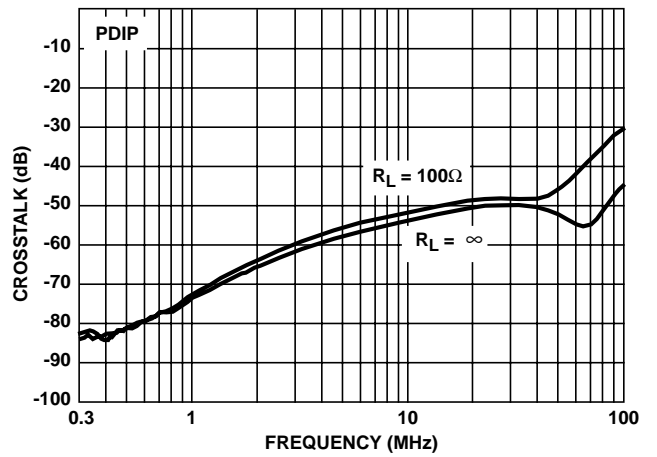
FIGURE 37. ALL HOSTILE CROSSTALK

intersil

Die Characteristics

DIE DIMENSIONS:

79 mils x 118 mils x 19 mils

2000μm x 3000μm x 483μm

METALLIZATION:

Type: Metal 1: AICu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AICu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

SUBSTRATE POTENTIAL (Powered Up):
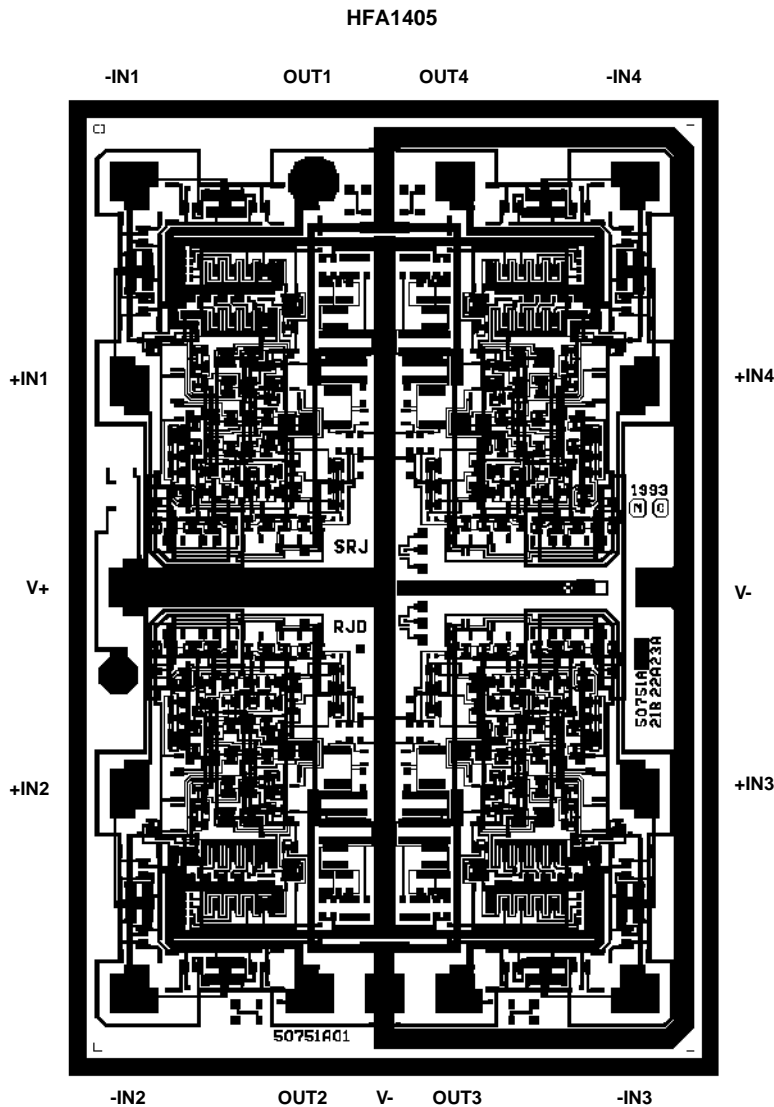
Floating (Recommend Connection to V-)

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

320

Metallization Mask Layout

HFA1405

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

For information regarding Intersil Corporation and its products, see web site **http://www.intersil.com**