

# CD54AC00F3A, CD54ACT00F3A

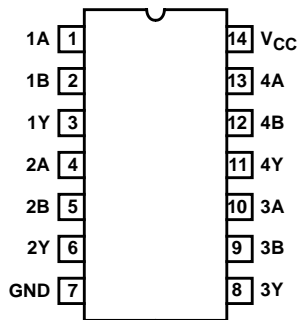
July 1998

## Quad 2-Input NAND Gate

### Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Exceeds 2kV ESD Protection MIL-STD-883, Method 3015
- Meets JEDEC Standard No. 20
- SCR - Latch-Up-Resistant CMOS Process and Circuit Design
- Speed of Bipolar FAST/A/S with Significantly Reduced Power Consumption
- Functionally and Pin-Compatible with Industry 54 Bipolar Types in the FAST, AS and S Series
- Balanced Propagation Delays
- Military Operating Temperature Range
  - Ceramic (CERDIP) 54 Series: ..... -55 to 125°C
- ±24mA Output Drive Current, Drives 75Ω Lines without Need for Terminations
- Fan Out (Over Temperature)
  - ACL Loads ..... 2400
  - FAST Loads..... 15
  - AS Loads..... 48
- Balanced Noise Immunity at 30% of Supply for AC Types
- Supply Voltage Range
  - AC Types ..... 1.5V to 5.5V
  - ACT Types ..... 4.5V to 5.5V

### Pinout



### Description

The CD54AC00F3A and CD54ACT00F3A are quad 2-input NAND gates that utilize the Harris Advanced CMOS Logic technology.

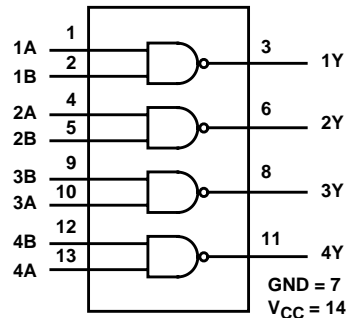
### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD54AC00F3A	-55 to 125	14 Ld CERDIP	F14.3
CD54ACT00F3A	-55 to 125	14 Ld CERDIP	F14.3

NOTE:

1. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

### Functional Diagram



TRUTH TABLE

INPUTS		OUTPUTS
A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

## CD54AC00F3A, CD54ACT00F3A

### Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 6V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 50mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 50mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ (Note 2) .....	$\pm 100mA$

### Thermal Information

Thermal Resistance (Typical, Note 4)	$\theta_{JA}$ ( $^{\circ}C/W$ )	$\theta_{JC}$ ( $^{\circ}C/W$ )
CERDIP Package .....	80	24
Maximum Junction Temperature (Hermetic Package or Die) ...	175 $^{\circ}C$	
Maximum Storage Temperature Range .....	-65 $^{\circ}C$ to 150 $^{\circ}C$	
Maximum Lead Temperature (Soldering 10s) .....	300 $^{\circ}C$	

### Operating Conditions

Temperature Range, $T_A$ .....	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, $V_{CC}$ (Note 3)	
AC Types .....	1.5V to 5.5V
ACT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I, V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Slew Rate, $dt/dv$	
AC Types	
1.5V to 3V .....	50ns (Max)
3.6V to 5.5V .....	20ns (Max)
4.5V to 5.5V .....	10ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

#### NOTES:

2. For up to 4 outputs per device, add  $\pm 25mA$  for each additional output.
3. Unless otherwise specified, all voltages are referenced to ground.
4.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

### DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS	
		$V_I$ (V)	$I_O$ (mA)		MIN	MAX	MIN	MAX		
<b>AC TYPES</b>										
High Level Input Voltage	$V_{IH}$	-	-	1.5	1.2	-	1.2	-	V	
				3	2.1	-	2.1	-	V	
				4.5	3.15 (Note 5)	-	3.15 (Note 5)	-	V	
				5.5	3.85	-	3.85	-	V	
Low Level Input Voltage	$V_{IL}$	-	-	1.5	-	0.3	-	0.3	V	
				3	-	0.9	-	0.9	V	
				4.5	-	1.35 (Note 5)	-	1.35 (Note 5)	V	
				5.5	-	1.65	-	1.65	V	
High Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.05	-0.05	1.5	1.4	-	1.4	-	V
			-0.05	-0.05	3	2.9	-	2.9	-	V
			-0.05	-0.05	4.5	4.4	-	4.4	-	V
			-4	-4	3	2.58	-	2.4	-	V
			-24	-24	4.5	3.94 (Note 5)	-	3.7 (Note 5)	-	V
			-50 (Note 6, 7)	-50	5.5	-	-	3.85	-	V

**CD54AC00F3A, CD54ACT00F3A**

**DC Electrical Specifications (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	MAX	MIN	MAX	
Low Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	1.5	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.5	V
			24	4.5	-	0.36 (Note 5)	-	0.5 (Note 5)	V
			50 (Note 6, 7)	5.5	-	-	-	1.65	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	-	5.5	-	±0.1 (Note 5)	-	±1 (Note 5)	µA
Quiescent Device Current	I <sub>CC</sub>		0	5.5	-	4 (Note 5)	-	80 (Note 5)	µA
<b>ACT TYPES</b>									
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2 (Note 5)	-	2 (Note 5)	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	0.8 (Note 5)	-	0.8 (Note 5)	V
High Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.05	4.5	4.4	-	4.4	-	V
			-24	4.5	3.94 (Note 5)	-	3.7 (Note 5)	-	V
			-50 (Note 6, 7)	5.5	-	-	3.85	-	V
Low Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.05	4.5	-	0.1	-	0.1	V
			24	4.5	-	0.36 (Note 5)	-	0.5 (Note 5)	V
			50 (Note 6, 7)	5.5	-	-	-	1.65	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	-	5.5	-	±0.1 (Note 5)	-	±1 (Note 5)	µA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	4 (Note 5)	-	80 (Note 5)	µA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	2.4	-	3	mA

**NOTES:**

5. Tested at 100%.
6. Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
7. Test verifies a minimum transmission-line-drive capability of 75Ω for 54AC/ACT Series.

**ACT Input Load Table**

INPUT	UNIT LOAD
All	0.15

NOTE: Unit load is ΔI<sub>CC</sub> limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

## CD54AC00F3A, CD54ACT00F3A

### Switching Specifications Input $t_r$ , $t_f = 3\text{ns}$ , $C_L = 50\text{pF}$ (Worst Case)

PARAMETER	SYMBOL	$V_{CC}$ (V)	-55°C TO 125°C			UNITS
			MIN	TYP	MAX	
<b>AC TYPES</b>						
Propagation Delay, Input to Output	$t_{PLH}$ , $t_{PHL}$	1.5	-	-	91	ns
		3.3 (Note 9)	3.1	-	10.2	ns
		5 (Note 10)	2.2	-	7.3 (Note 8)	ns
Input Capacitance	$C_I$	-	-	-	10	pF
Power Dissipation Capacitance	$C_{PD}$ (Note 11)	-	-	45	-	pF
<b>ACT TYPES</b>						
Propagation Delay, Input to Output	$t_{PLH}$	5 (Note 10)	3.2	-	10.8 (Note 8)	ns
	$t_{PHL}$					4
Input Capacitance	$C_I$	-	-	-	10	pF
Power Dissipation Capacitance	$C_{PD}$ (Note 11)	-	-	45	-	pF

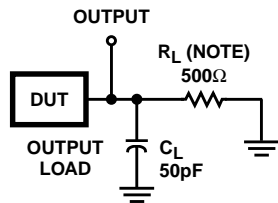
**NOTES:**

8. Limits tested at 100%.
9. 3.3V Min at 3.6V, Max at 3V.
10. 5V Min at 5.5V, Max at 4.5V
11.  $C_{PD}$  is used to determine the dynamic power consumption per gate.  
 AC:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$   
 ACT:  $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

### Burn-In Test Circuit Connections (Use DC II for F3A Burn-In and AC for Life Test)

DC	DC BURN-IN I			DC BURN-IN II		
	OPEN	GROUND	$V_{CC}$ (6V)	OPEN	GROUND	$V_{CC}$ (6V)
CD54AC/ACT00	3, 6, 8, 11	1, 2, 4, 5, 7, 9, 10, 12, 13	14	3, 6, 8, 11	7	1, 2, 4, 5, 9, 10, 12 - 14
AC	OPEN	GROUND	$1/2 V_{CC}$ (3V)	$V_{CC}$ (6V)	OSCILLATOR	
					50kHz	25kHz
CD54AC/ACT00	-	7	3, 6, 8, 11	14	1, 2, 4, 5, 9, 10, 12, 13	-

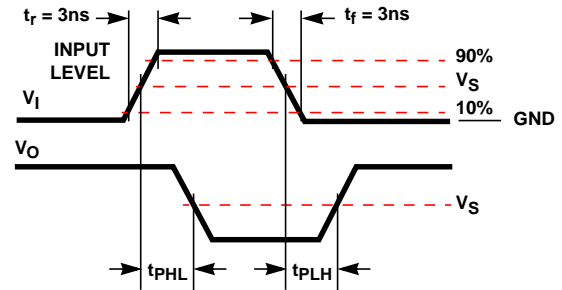
NOTE: Each pin except  $V_{CC}$  and Gnd will have a resistor of  $2\text{k}\Omega$ - $47\text{k}\Omega$ .



NOTE: For AC Series Only: When  $V_{CC} = 1.5\text{V}$ ,  $R_L = 1\text{k}\Omega$ .

	CD54AC	CD54ACT
Input Level	$V_{CC}$	3V
Input Switching Voltage, $V_S$	$0.5 V_{CC}$	1.5V
Output Switching Voltage, $V_S$	$0.5 V_{CC}$	$0.5 V_{CC}$

**FIGURE 1. PROPAGATION DELAY TIMES**



**FIGURE 2. WAVEFORMS**