

**COMPLETE DATA SHEET  
COMING SOON!**

June 1997

## Dual "J-K" Flip-Flop with Set and Reset

### Description

The CD54AC109/3A and CD54ACT109/3A are dual "J-K" flip-flops with set and reset that utilize the Harris Advanced CMOS Logic technology. These flip-flops have independent J,  $\bar{K}$ ,  $\overline{\text{Set}}$ ,  $\overline{\text{Reset}}$  and Clock inputs and Q and  $\bar{Q}$  outputs. The CD54AC109/3A and CD54ACT109/3A changes state on the positive-going transition of the clock.  $\overline{\text{Set}}$  and  $\overline{\text{Reset}}$  are accomplished asynchronously by low-level inputs.

The CD54AC109/3A and CD54ACT109/3A are supplied in 16 lead dual-in-line ceramic packages (F suffix).

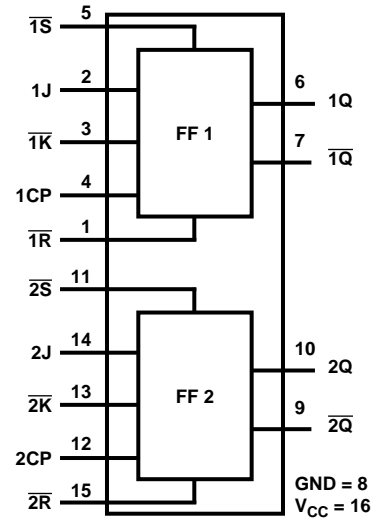
**ACT INPUT LOAD TABLE**

| INPUT                         | UNIT LOAD (NOTE 1) |
|-------------------------------|--------------------|
| J, CP, $\overline{\text{CP}}$ | 1                  |
| $\bar{K}$                     | 0.53               |
| $\bar{S}$ , $\bar{R}$         | 0.58               |

NOTE:

- Unit load is  $\Delta I_{CC}$  limit specified in DC Electrical Specifications Table, e.g., 2.4mA Max at +25°C.

### Functional Diagram



### Absolute Maximum Ratings

DC Supply Voltage,  $V_{CC}$  ..... -0.5V to +6V  
 DC Input Diode Current,  $I_{IK}$   
 For  $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$  .....  $\pm 20mA$   
 DC Output Diode Current,  $I_{OK}$   
 For  $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$  .....  $\pm 50mA$   
 DC Output Source or Sink Current, Per Output Pin,  $I_O$   
 For  $V_O > -0.5V$  or  $V_O < V_{CC} + 0.5V$  .....  $\pm 50mA$   
 DC  $V_{CC}$  or GND Current,  $I_{CC}$  or  $I_{GND}$   
 For Up to 4 Outputs Per Device, Add  $\pm 25mA$  For Each  
 Additional Output .....  $\pm 100mA$

Power Dissipation Per Package,  $P_D$   
 $T_A = -55^\circ C$  to  $+100^\circ C$  (Package F) ..... 500mW  
 $T_A = +100^\circ C$  to  $+125^\circ C$  (Package F) ..... Derate Linearly at  
 8mW/ $^\circ C$  to 300mW  
 Operating Temperature Range,  $T_A$   
 Package Type F .....  $-55^\circ C$  to  $+125^\circ C$   
 Storage Temperature,  $T_{STG}$  .....  $-65^\circ C$  to  $+150^\circ C$   
 Lead Temperature (During Soldering)  
 At Distance 1/16in.  $\pm$  1/32in. (1.59mm  $\pm$  0.79mm)  
 From Case For 10s Max .....  $+265^\circ C$   
 Unit Inserted Into a PC Board (Min Thickness 1/16in., 1.59mm)  
 With Solder Contacting Lead Tips Only .....  $+300^\circ C$

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### Recommended Operating Conditions

Supply Voltage Range,  $V_{CC}$   
 Unless Otherwise Specified, All Voltages Referenced to GND  
 $T_A$  = Full Package Temperature Range  
 CD54AC Types ..... 1.5V to 5.5V  
 CD54ACT Types ..... 4.5V to 5.5V  
 DC Input or Output Voltage,  $V_I$ ,  $V_O$  ..... 0V to  $V_{CC}$

Operating Temperature,  $T_A$  .....  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise and Fall Slew Rate,  $dt/dv$   
 at 1.5V to 3V (AC Types) ..... 0ns/V to 50ns/V  
 at 3.6V to 5.5V (AC Types) ..... 0ns/V to 20ns/V  
 at 4.5V to 5.5V (AC Types) ..... 0ns/V to 10ns/V