Data Sheet July 1999 File Number 3951.3

60A, 30V, 0.027 Ohm, P-Channel Power MOSFETs

These P-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA49045.

Ordering Information

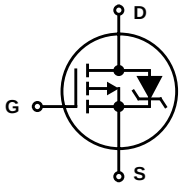
PART NUMBER	PACKAGE	BRAND
RFG60P03	TO-247	RFG60P03
RFP60P03	TO-220AB	RFP60P03
RF1S60P03SM	TO-263AB	F1S60P03

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in tape and reel, i.e. RF1S60P03SM9A.

Features

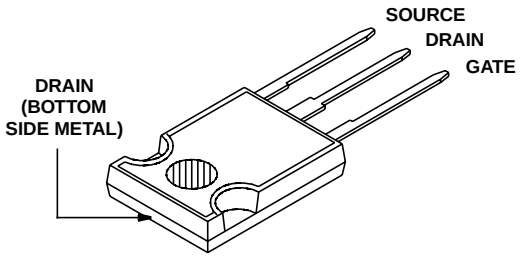
- 60A, 30V
- $r_{DS(ON)} = 0.027\Omega$
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175^{o}C Operating Temperature
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

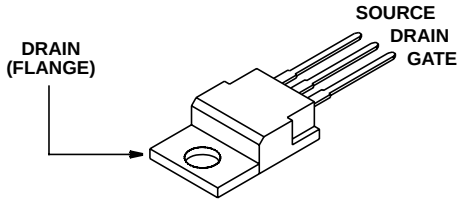


Packaging

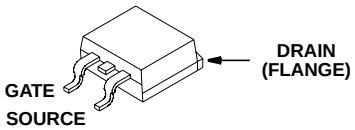
JEDEC STYLE TO-247



JEDEC TO-220AB



JEDEC TO-263AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFG60P03, RFP60P03, RFS60P03SM	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	-30	V
Drain to Gate Voltage, (R_{gs} = 20kΩ) (Note 1)	V_{DGR}	-30	V
Gate to Source Voltage	V_{GS}	±20	V
Continuous Drain Current (Figure 2)	I_D	60	A
Pulsed Drain Current (Note 3)	I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating	E_{AS}	Figure 6	
Maximum Power Dissipation (Figure 1)	P_D	176	W
Derate Above 25^oC		1.17	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V (Figure 11)		-30	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250µA (Figure 10)		-2	-	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V		-	-	-1	µA
		V_{DS} = 0.8 x Rated BV_{DSS}, $T_C = 150^oC$		-	-	-50	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 60A, V_{GS} = 10V		-	-	0.027	Ω
Turn-On Time	t_{ON}	V_{DD} = 15V, $I_D \approx$ 60A, R_L = 0.25Ω, V_{GS} = -10V, R_G = 2.5Ω, (Figure 13)		-	-	140	ns
Turn-On Delay Time	$t_{d(ON)}$			-	20	-	ns
Rise Time	t_r			-	75	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	35	-	ns
Fall Time	t_f			-	40	-	ns
Turn-Off Time	t_{OFF}			-	-	115	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0 to -20V	V_{DD} = -24V, $I_D \approx$ 60A, R_L = 0.4Ω, $I_{g(REF)}$ = -3mA	-	190	230	nC
Gate Charge at 10V	$Q_{g(-10)}$	V_{GS} = 0 to -10V		-	100	120	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0 to -2V		-	7.5	9	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 12)		-	3000	-	pF
Output Capacitance	C_{OSS}			-	1500	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	525	-	pF
Thermal Resistance, Junction to Case	$R_{\theta JC}$	(Figure 3)		-	-	0.85	$^oC/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	TO-220AB, TO- 263AB		-	-	62	$^oC/W$
		TO-247		-	-	30	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = -60A	-	-	-1.75	V
Diode Reverse Recovery Time	t_{rr}	I_{SD} = -60A, dI_{SD}/dt = 100A/µs	-	-	200	ns

NOTE:

2. Pulse test: pulse width ≤ 300µs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3)

Typical Performance Curves Unless Otherwise Specified

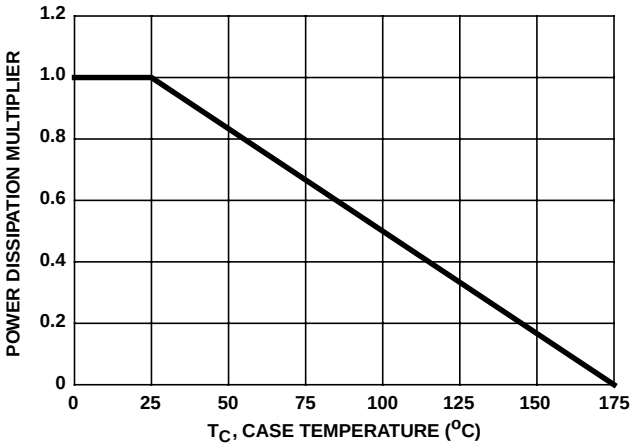


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

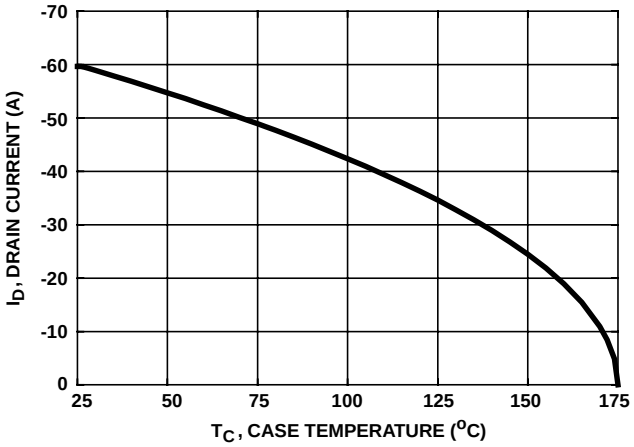


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

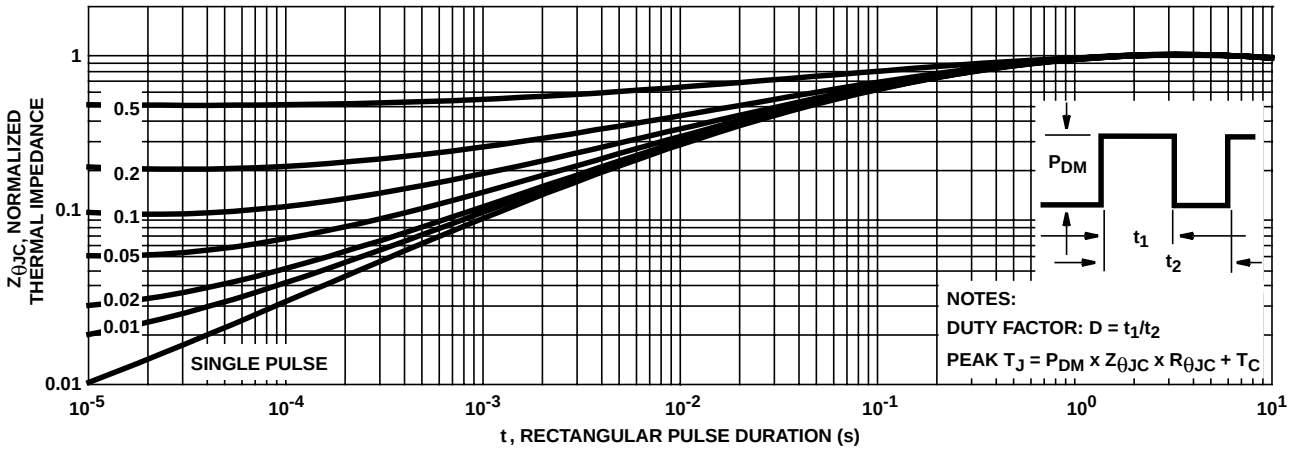


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

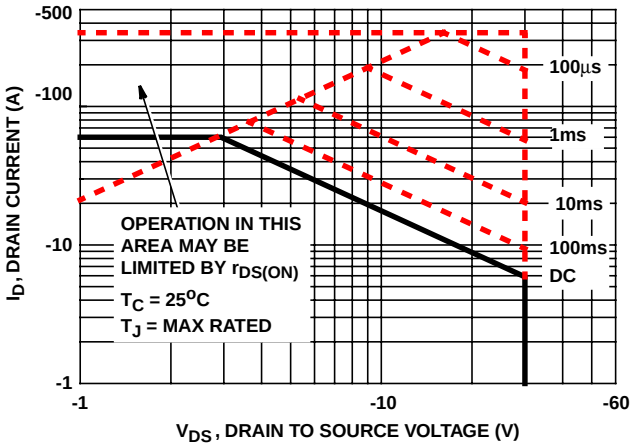


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

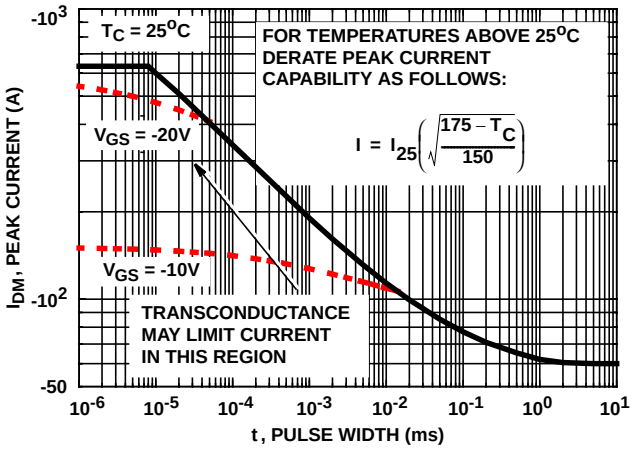
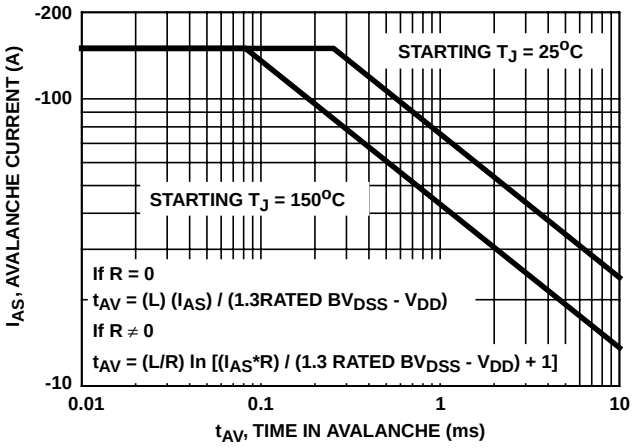


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING

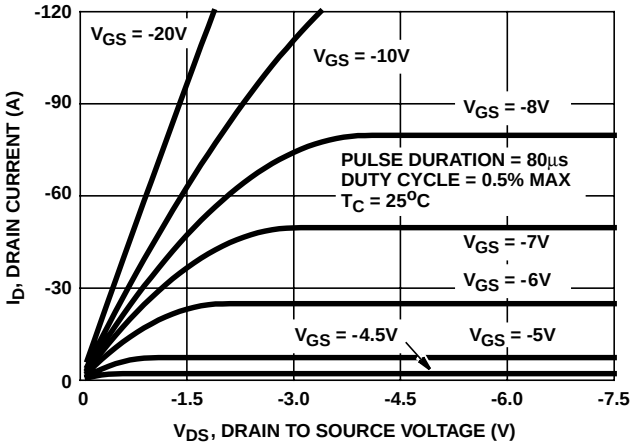


FIGURE 7. SATURATION CHARACTERISTICS

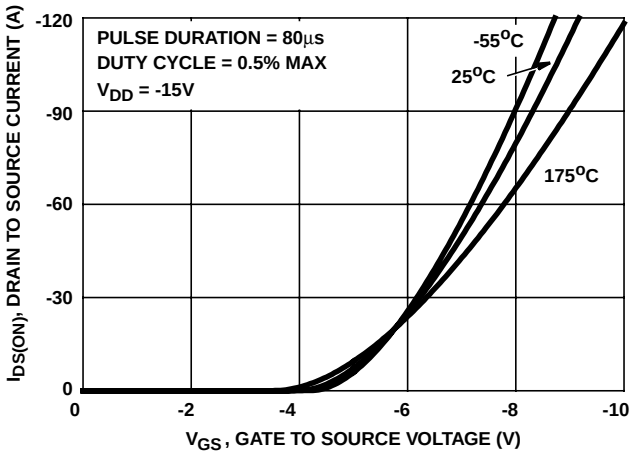


FIGURE 8. TRANSFER CHARACTERISTICS

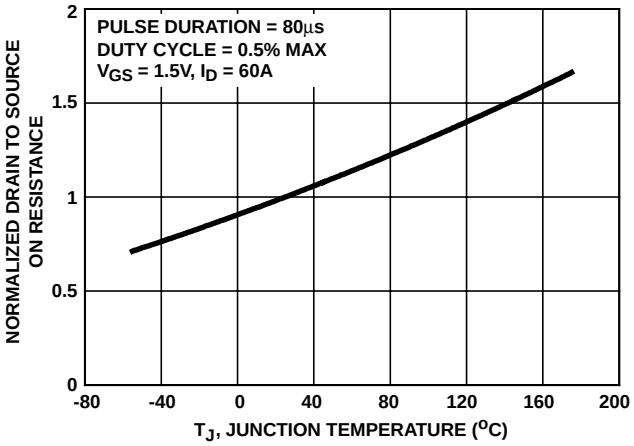


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

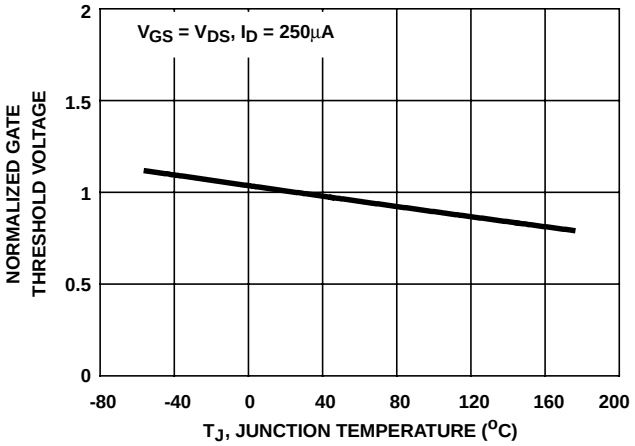


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

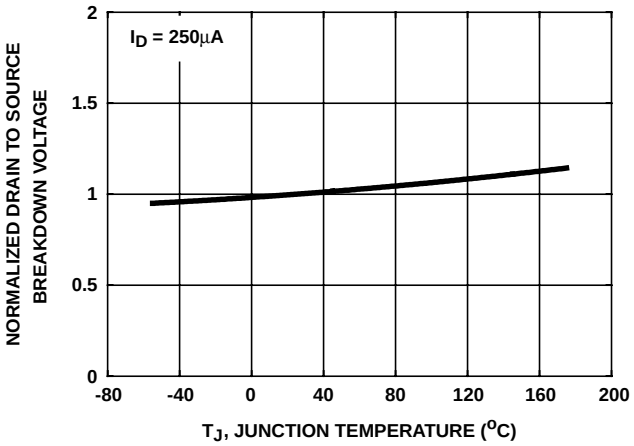


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

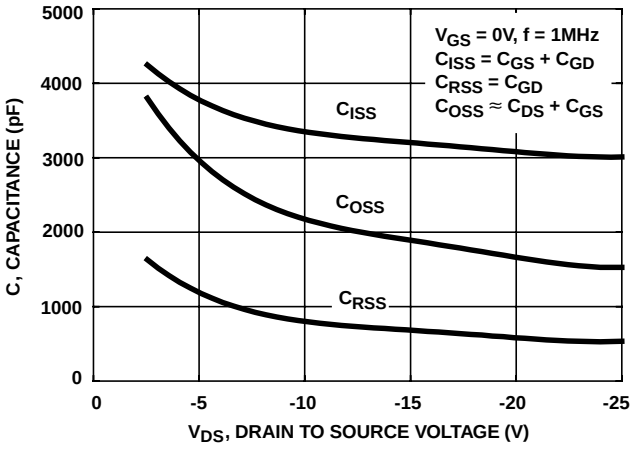
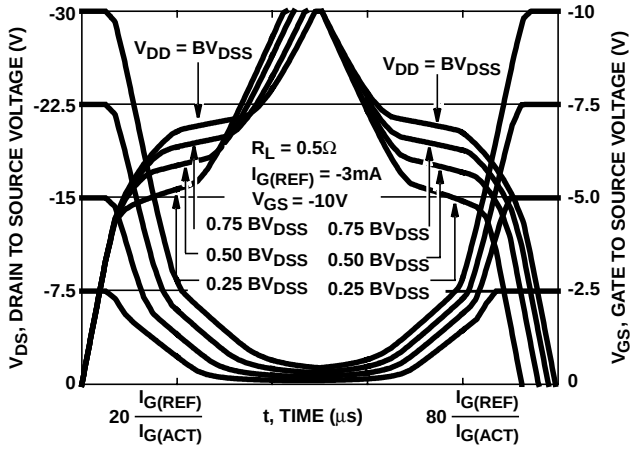


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

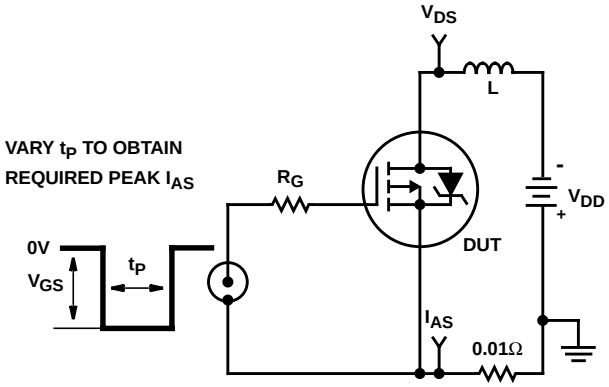


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

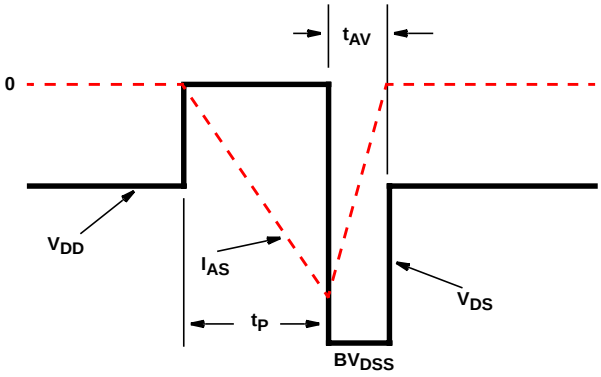


FIGURE 15. UNCLAMPED ENERGY WAVEFORM

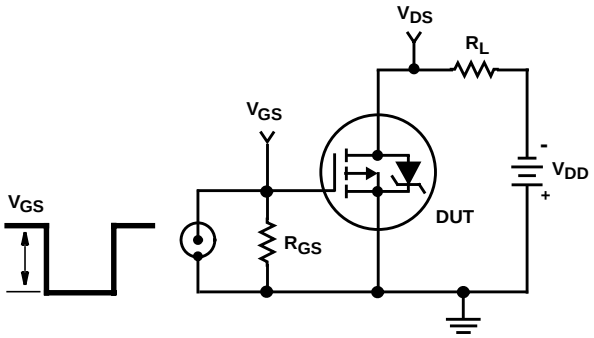


FIGURE 16. SWITCHING TIME TEST CIRCUIT

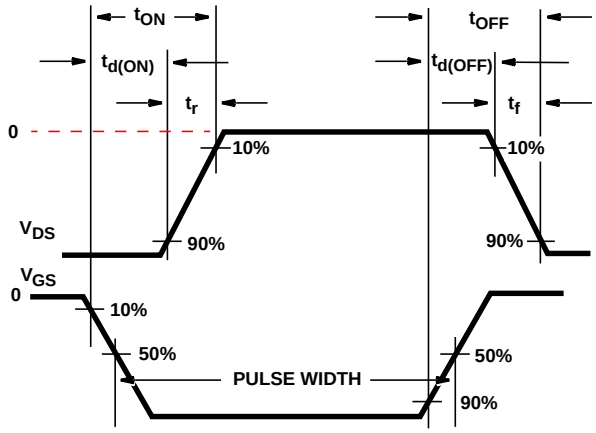


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

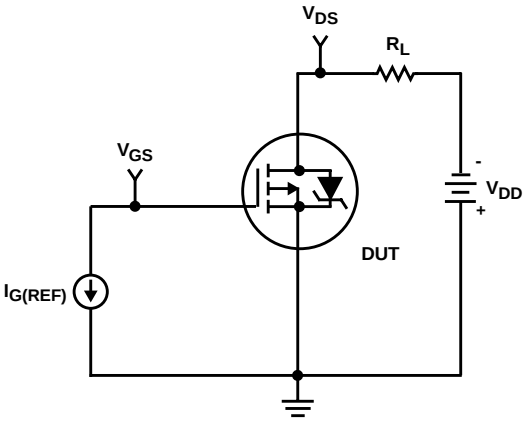


FIGURE 18. GATE CHARGE TEST CIRCUIT

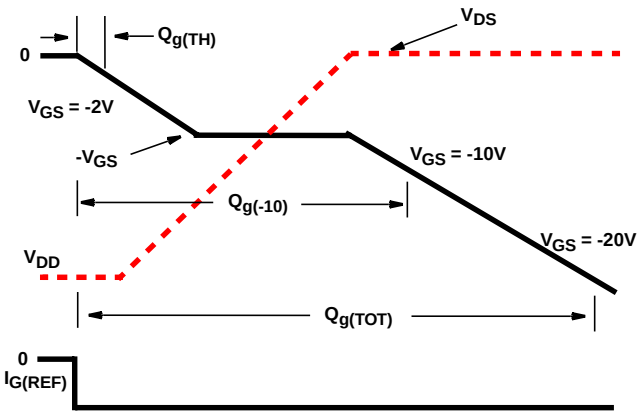


FIGURE 19. GATE CHARGE WAVEFORMS

PSPICE Electrical Model

.SUBCKT RFP60P03 2 1 3 REV 6/21/94

CA 12 8 5.01e-9
CB 15 14 3.9e-9
CIN 6 8 3.09e-9

DBODY 5 7 DBDMOD
DBREAK 7 11 DBKMOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -36.59
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTO 20 6 8 18 1

IT 8 17 1

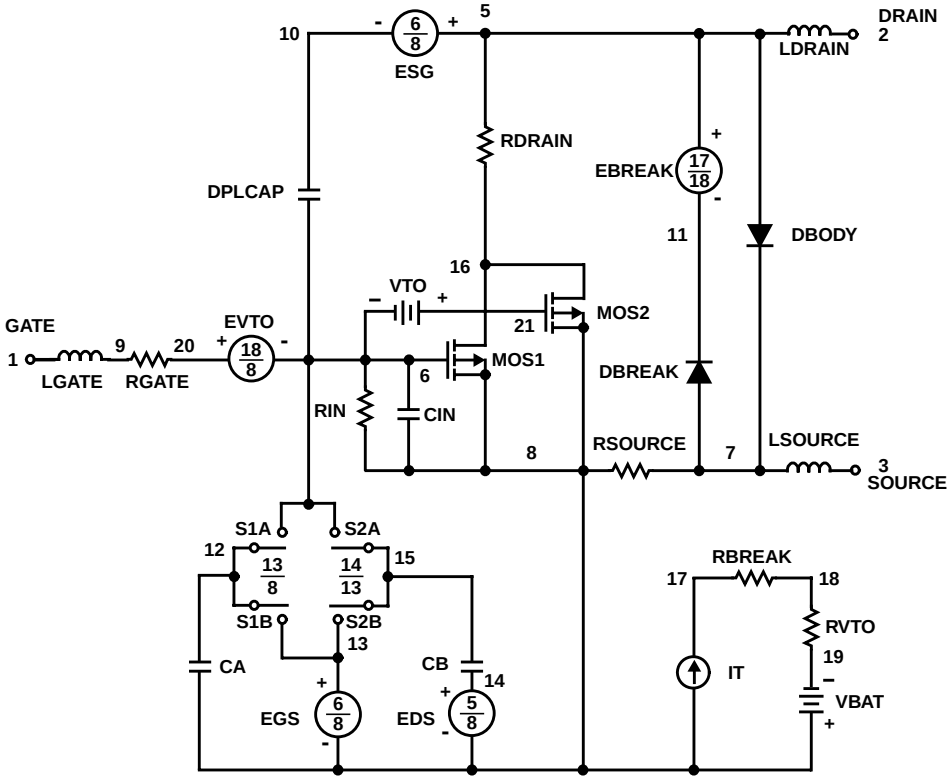
LDRAIN 2 5 1e-9
LGATE 1 9 4.92e-9
LSOURCE 3 7 2.36e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 1e-4
RGATE 9 20 3.25
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 11.28e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 -0.92



.MODEL DBDMOD D (IS=4.21e-13 RS=1e-2 TRS1=-2.69e-4 TRS2=-1.33e-6 CJO=5.05e-9 TT=5.33e-8)
.MODEL DBKMOD D (RS=3.80e-2 TRS1=-4.76e-4 TRS2=-4.17e-12)
.MODEL DPLCAPMOD D (CJO=4.05e-9 IS=1e-30 N=10)
.MODEL MOSMOD PMOS (VTO=-3.98 KP=16.27 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=8.05e-4 TC2=1.48e-6)
.MODEL RDSMOD RES (TC1=2.80e-3 TC2=2.62e-6)
.MODEL RVTOMOD RES (TC1=-3.34e-3 TC2=1.46e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=7.5 VOFF=4.5)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=4.5 VOFF=7.5)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=1.43 VOFF=-3.57)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.57 VOFF=1.43)

.ENDS

NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; authors, William J. Hepp and C. Frank Wheatley.