Data Sheet August 1999 File Number 3968.5

## 3.5A/2.5A, 12V, 0.050/0.130 Ohm, Logic Level, Complementary LittleFET™ Power MOSFET

This complementary power MOSFET is manufactured using an advanced MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It is designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and low voltage bus switches. This product achieves full rated conduction at a gate bias in the 3V to 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

Formerly developmental type TA49092.

## Ordering Information

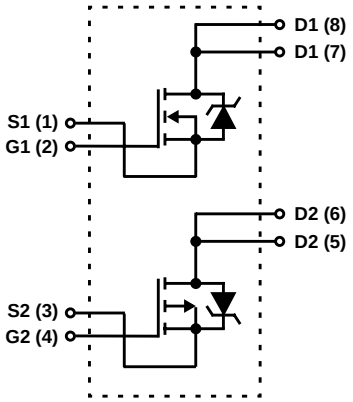
| PART NUMBER | PACKAGE | BRAND |
|---|---|---|
| RF1K49092 | MS-012AA | RF1K49092 |

NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e., RF1K4909296.

## Features

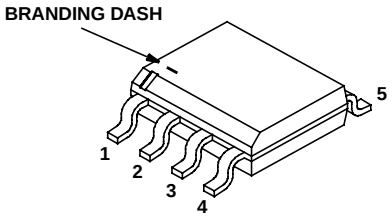
- 3.5A, 12V (N-Channel)
  2.5A, 12V (P-Channel)
- $r_{DS(ON)}$ = 0.050Ω (N-Channel)
  $r_{DS(ON)}$ = 0.130Ω (P-Channel)
- Temperature Compensating PSPICE® Model
- On-Resistance vs Gate Drive Voltage Curves
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

## Symbol




## Packaging

JEDEC MS-012AA



## Absolute Maximum Ratings $T_A = 25^oC$ Unless Otherwise Specified

| | N-CHANNEL | P-CHANNEL | UNITS |
|---|---|---|---|
| Drain to Source Voltage (Note 1) . . . . . $V_{DSS}$ | 12 | -12 | V |
| Drain to Gate Voltage ($R_{GS}$ = 20kΩ, Note 1) . . . . . $V_{DGR}$ | 12 | -12 | V |
| Gate to Source Voltage . . . . . $V_{GS}$ | ±10 | ±10 | V |
| Drain Current | | | |
| Continuous (Pulse Width = 5s) . . . . . $I_D$ | 3.5 | 2.5 | A |
| Pulsed (Figures 5, 26) . . . . . $I_{DM}$ | Refer to Peak Current Curve | Refer to Peak Current Curve | |
| Pulsed Avalanche Rating (Figures 6, 27) . . . . . $E_{AS}$ | Refer to UIS Curve | Refer to UIS Curve | |
| Power Dissipation | | | |
| $T_A = 25^oC$ . . . . . $P_D$ | 2 | 2 | W |
| Derate Above $25^oC$ . . . . . | 0.016 | 0.016 | $W/^oC$ |
| Operating and Storage Temperature . . . . . $T_J$, $T_{STG}$ | -55 to 150 | -55 to 150 | $^oC$ |
| Maximum Temperature for Soldering | | | |
| Leads at 0.063in (1.6mm) from Case for 10s . . . . . $T_L$ | 300 | 300 | $^oC$ |
| Package Body for 10s, See Techbrief 334 . . . . . $T_{pkg}$ | 260 | 260 | $^oC$ |

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. $T_J = 25^oC$ to $125^oC$.

## N-Channel Electrical Specifications $T_A = 25^oC$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Drain to Source Breakdown Voltage | $BV_{DSS}$ | $I_D$ = 250µA, $V_{GS}$ = 0V, (Figure 13) | | 12 | - | - | V |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS} = V_{DS}$, $I_D$ = 250µA, (Figure 12) | | 1 | - | 2 | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 12V, $V_{GS}$ = 0V | $T_A = 25^oC$ | - | - | 1 | µA |
| | | | $T_A = 150^oC$ | - | - | 50 | µA |
| Gate to Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±10V | | - | - | ±100 | nA |
| Drain to Source On Resistance | $r_{DS(ON)}$ | $I_D$ = 3.5A, $V_{GS}$ = 5V, (Figures 9, 11) | | - | - | 0.050 | Ω |
| Turn-On Time | $t_{ON}$ | $V_{DD}$ = 6V, $I_D \approx$ 3.5A, $R_L$ = 1.71Ω, $V_{GS}$ = 5V, $R_{GS}$ = 25Ω (Figure 10) | | - | - | 100 | ns |
| Turn-On Delay Time | $t_{d(ON)}$ | | | - | 18 | - | ns |
| Rise Time | $t_r$ | | | - | 60 | - | ns |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | - | 50 | - | ns |
| Fall Time | $t_f$ | | | - | 60 | - | ns |
| Turn-Off Time | $t_{OFF}$ | | | - | - | 140 | ns |
| Total Gate Charge | $Q_{g(TOT)}$ | $V_{GS}$ = 0V to 10V | $V_{DD}$ = 9.6V, $I_D$ = 3.5A, $R_L$ = 2.74Ω (Figure 15) | - | 20 | 25 | nC |
| Gate Charge at 5V | $Q_{g(5)}$ | $V_{GS}$ = 0V to 5V | | - | 12 | 15 | nC |
| Threshold Gate Charge | $Q_{g(TH)}$ | $V_{GS}$ = 0V to 1V | | - | 0.9 | 1.2 | nC |
| Input Capacitance | $C_{ISS}$ | $V_{DS}$ = 10V, $V_{GS}$ = 0V, f = 1MHz (Figure 14) | | - | 750 | - | pF |
| Output Capacitance | $C_{OSS}$ | | | - | 700 | - | pF |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | - | 275 | - | pF |
| Thermal Resistance Junction to Ambient | $R_{\theta JA}$ | Pulse width = 1s<br>Device mounted on FR-4 material | | - | - | 62.5 | $^oC/W$ |

## N-Channel Source to Drain Diode Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Source to Drain Voltage | $V_{SD}$ | $I_{SD}$ = 3.5A | - | - | 1.25 | V |
| Reverse Recovery Time | $t_{rr}$ | $I_{SD}$ = 3.5A, $dI_{SD}/dt$ = 100A/µs | - | - | 70 | ns |

## P-Channel Electrical Specifications $T_A = 25^oC$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Drain to Source Breakdown Voltage | $BV_{DSS}$ | $I_D$ = 250µA, $V_{GS}$ = 0V, (Figure 34) | | -12 | - | - | V |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS} = V_{DS}$, $I_D$ = 250µA, (Figure 33) | | -1 | - | -2 | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = -12V, $V_{GS}$ = 0V | $T_A = 25^oC$ | - | - | -1 | µA |
| | | | $T_A = 150^oC$ | - | - | -50 | µA |
| Gate to Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±10V | | - | - | ±100 | nA |
| Drain to Source On Resistance | $r_{DS(ON)}$ | $I_D$ = 2.5A, $V_{GS}$ = -5V | | - | - | 0.130 | Ω |
| Turn-On Time | $t_{ON}$ | $V_{DD}$ = -6V, $I_D \approx$ 2.5A, $R_L$ = 2.40Ω, $V_{GS}$ = -5V, $R_{GS}$ = 25Ω (Figure 31) | | - | - | 115 | ns |
| Turn-On Delay Time | $t_{d(ON)}$ | | | - | 25 | - | ns |
| Rise Time | $t_r$ | | | - | 65 | - | ns |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | - | 40 | - | ns |
| Fall Time | $t_f$ | | | - | 45 | - | ns |
| Turn-Off Time | $t_{OFF}$ | | | - | - | 110 | ns |
| Total Gate Charge | $Q_{g(TOT)}$ | $V_{GS}$ = 0V to -10V | $V_{DD}$ = -9.6V, $I_D$ = 2.5A, $R_L$ = 3.84Ω (Figure 36) | - | 19 | 24 | nC |
| Gate Charge at -5V | $Q_{g(-5)}$ | $V_{GS}$ = 0V to -5V | | - | 10 | 14 | nC |
| Threshold Gate Charge | $Q_{g(TH)}$ | $V_{GS}$ = 0V to -1V | | - | 0.8 | 1.1 | nC |
| Input Capacitance | $C_{ISS}$ | $V_{DS}$ = -10V, $V_{GS}$ = 0V, f = 1MHz (Figure 35) | | - | 775 | - | pF |
| Output Capacitance | $C_{OSS}$ | | | - | 550 | - | pF |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | - | 150 | - | pF |
| Thermal Resistance Junction-to-Ambient | $R_{\theta JA}$ | Pulse width = 1s, Device mounted on FR-4 material | | - | - | 62.5 | $^oC/W$ |

## P-Channel Source to Drain Diode Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Source to Drain Voltage | $V_{SD}$ | $I_{SD}$ = -2.5A | - | - | -1.25 | V |
| Reverse Recovery Time | $t_{rr}$ | $I_{SD}$ = -2.5A, $dI_{SD}/dt$ = -100A/µs | - | - | 55 | ns |

## *Typical Performance Curves (N-Channel)*

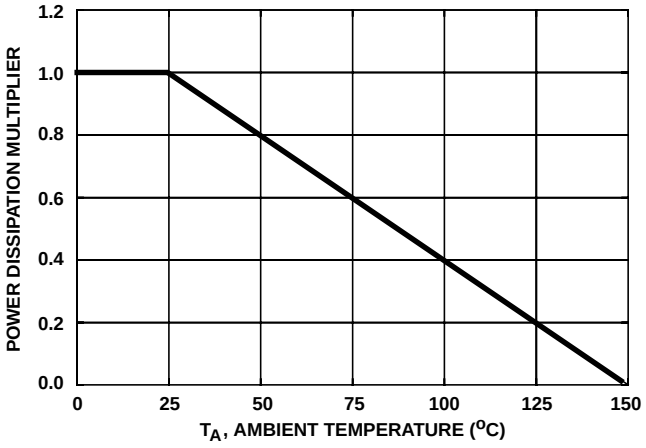



**FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE**

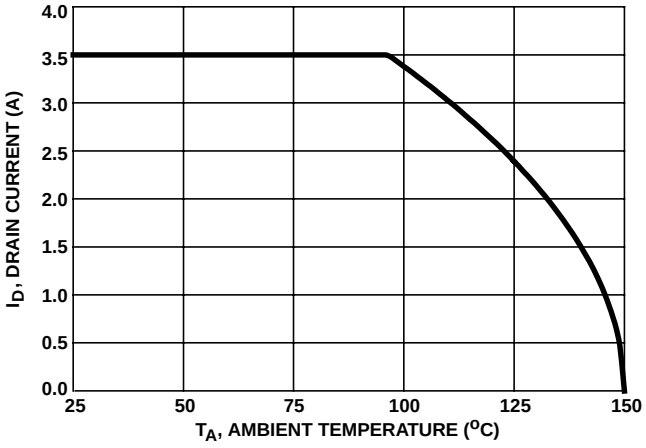



**FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE**

## Typical Performance Curves (N-Channel) (Continued)

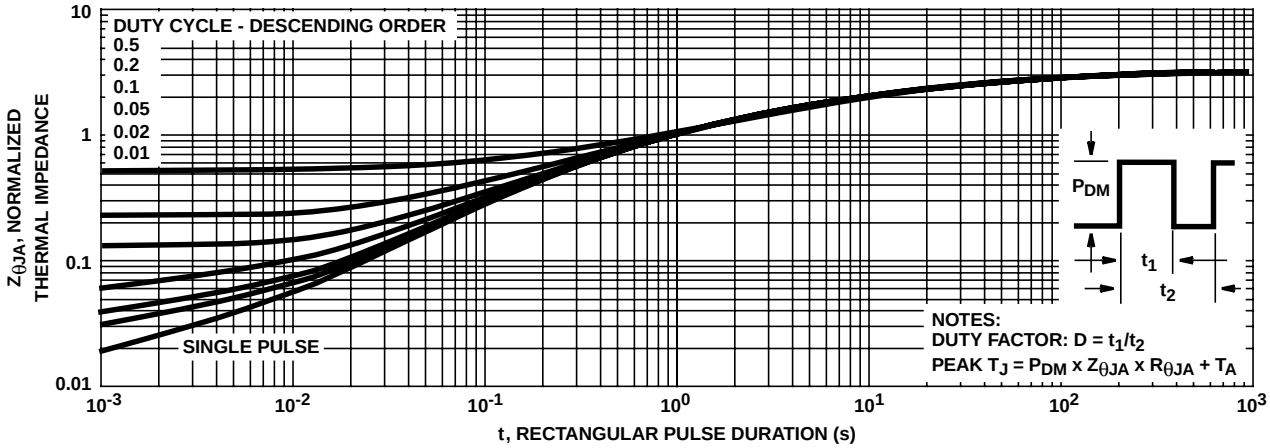



FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

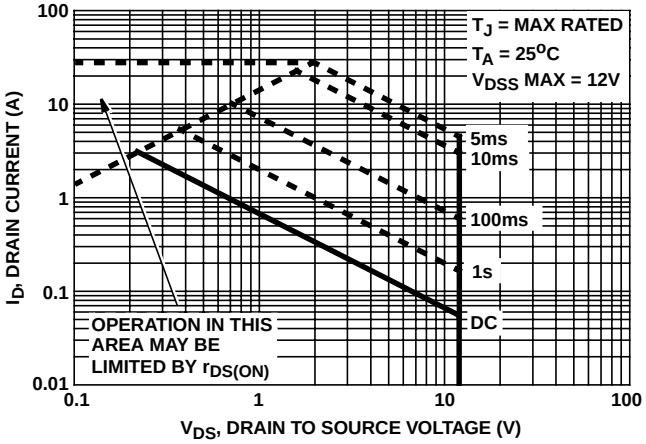



FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

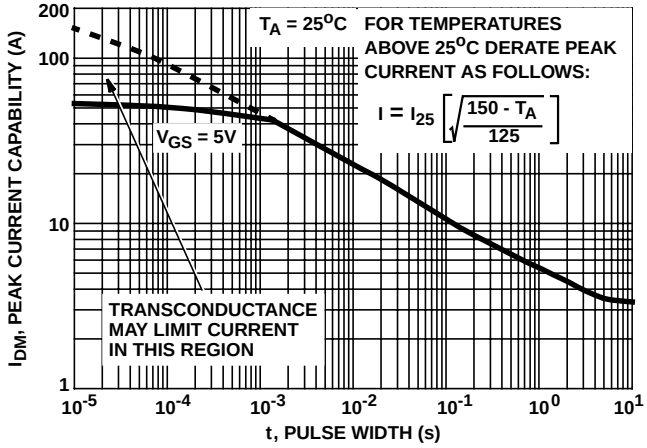
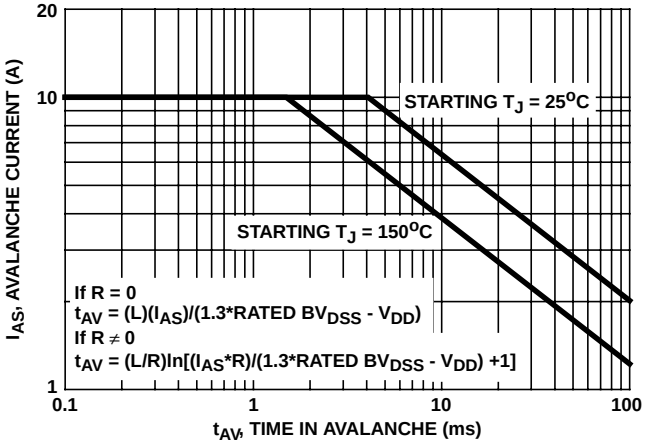



FIGURE 5. PEAK CURRENT CAPABILITY




NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

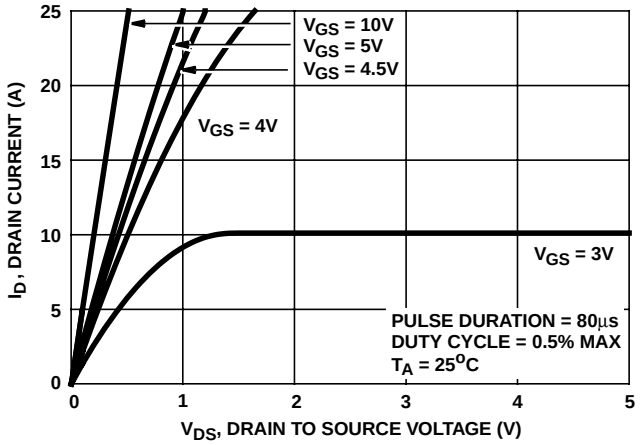



FIGURE 7. SATURATION CHARACTERISTICS

## Typical Performance Curves (N-Channel) (Continued)

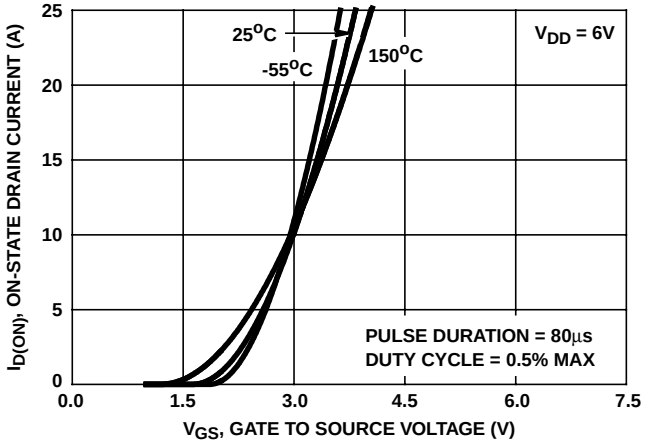



FIGURE 8. TRANSFER CHARACTERISTICS

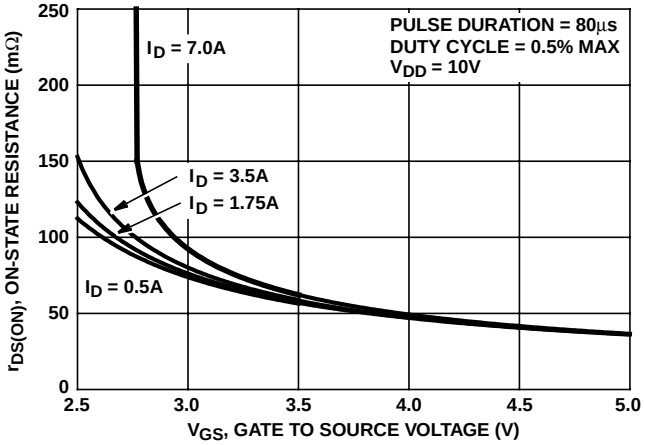



FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

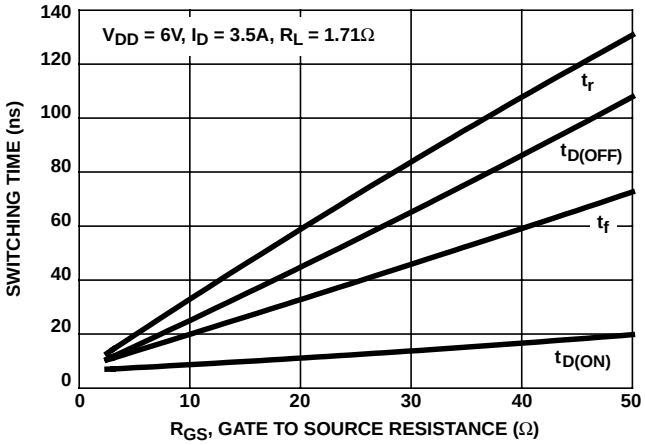



FIGURE 10. SWITCHING TIME vs GATE RESISTANCE

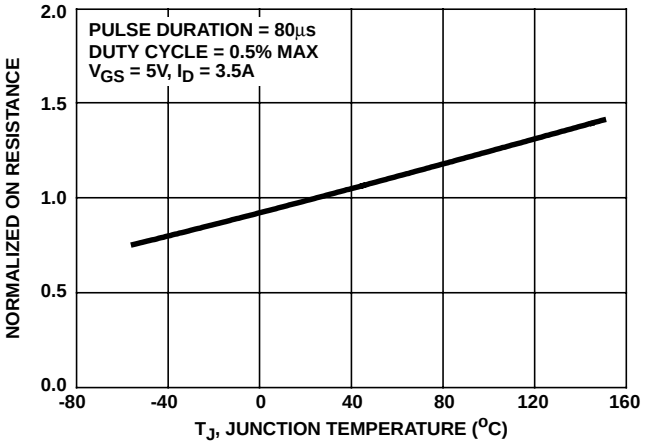



FIGURE 11. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

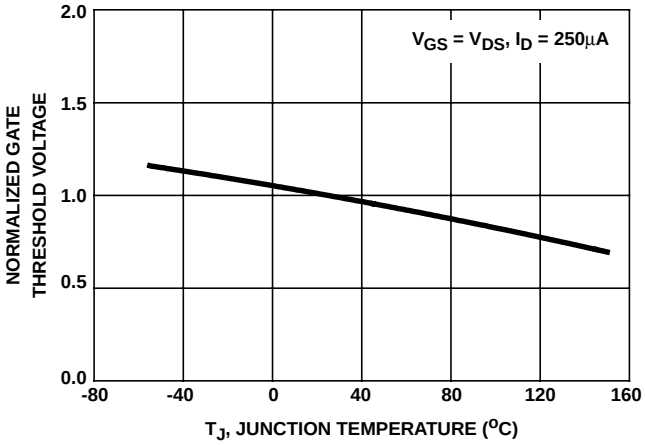



FIGURE 12. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

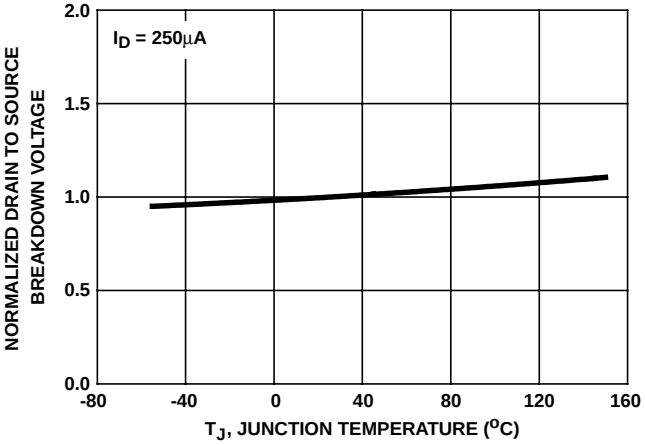



FIGURE 13. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

## Typical Performance Curves (N-Channel) (Continued)

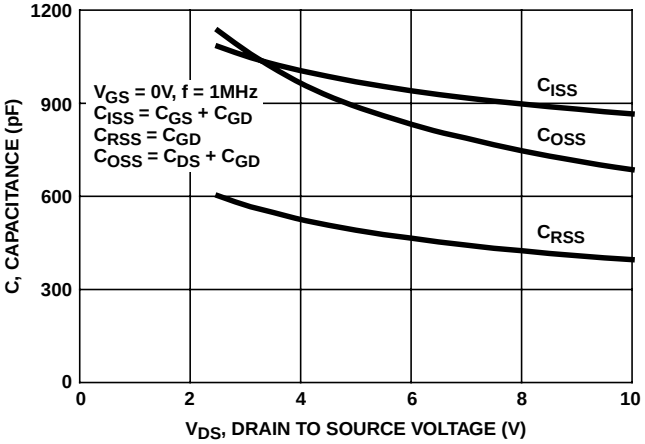
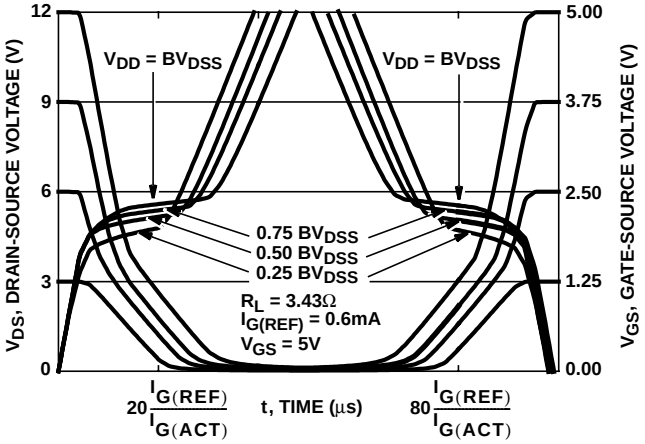



FIGURE 14. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE




NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 15. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

## Test Circuits and Waveforms (N-Channel)

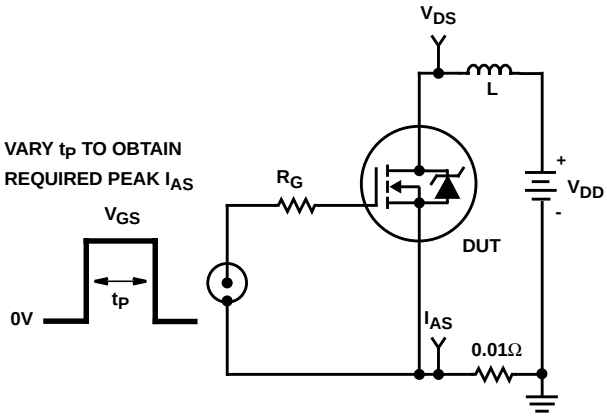



FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

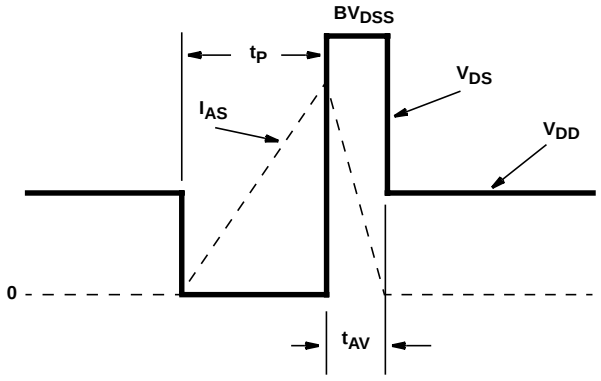



FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

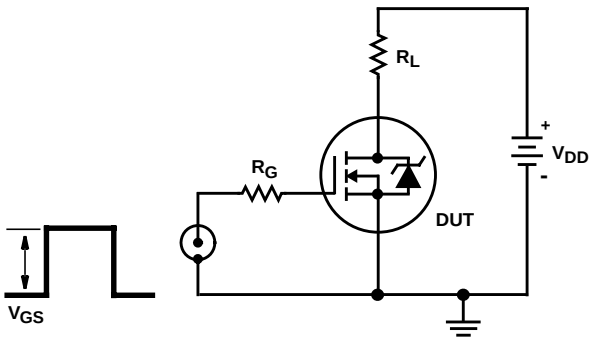



FIGURE 18. SWITCHING TIME TEST CIRCUIT

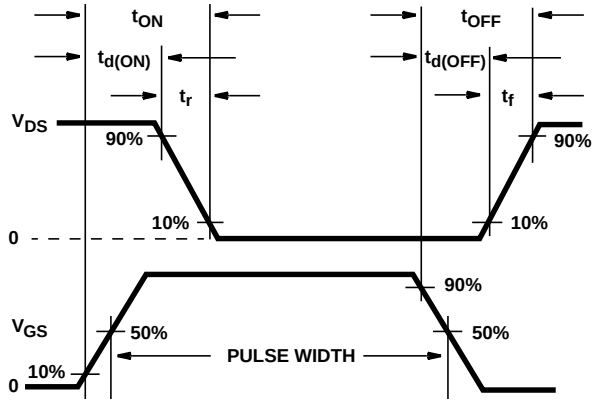



FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

## Test Circuits and Waveforms (N-Channel) (Continued)

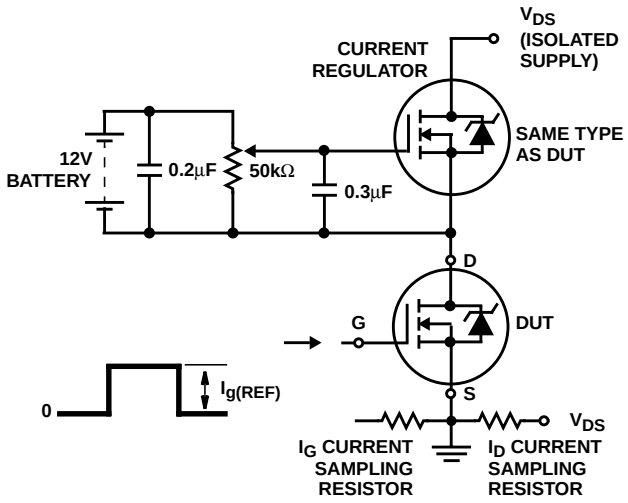



FIGURE 20. GATE CHARGE TEST CIRCUIT

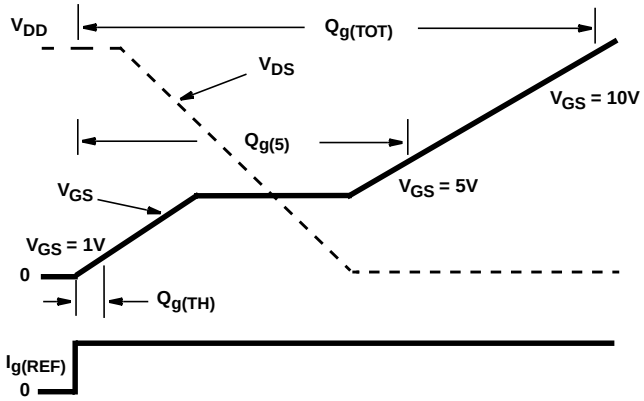



FIGURE 21. GATE CHARGE WAVEFORMS

## Typical Performance Curves (P-Channel)

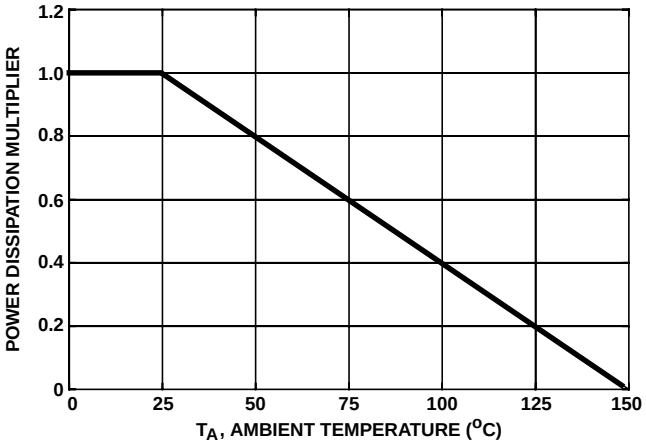



FIGURE 22. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

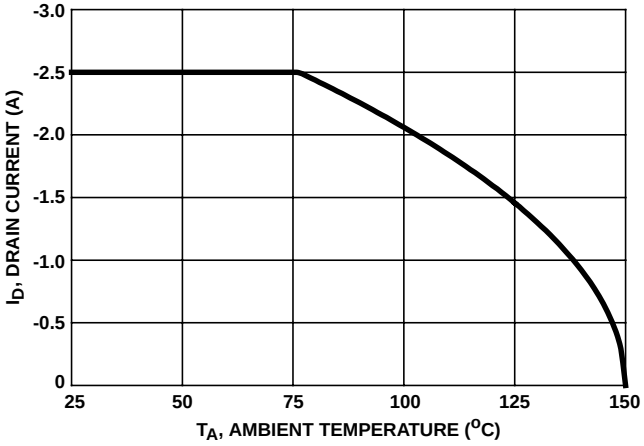



FIGURE 23. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

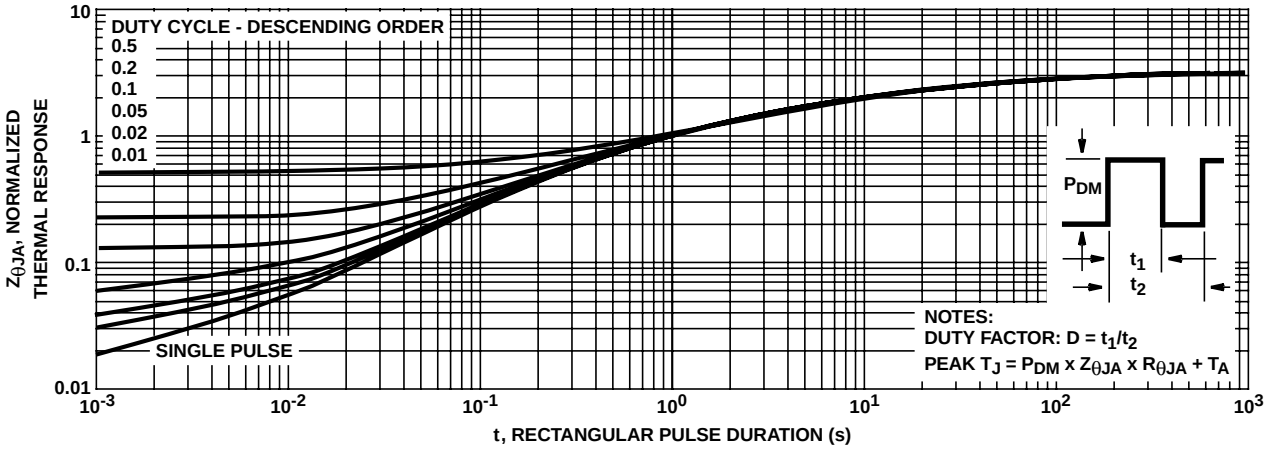



FIGURE 24. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

## Typical Performance Curves (P-Channel) (Continued)

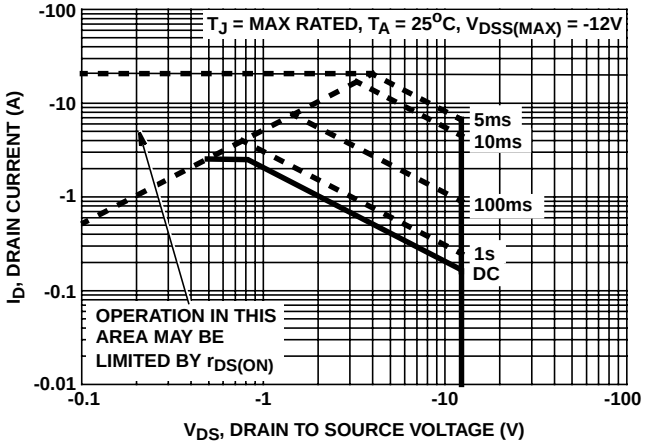



FIGURE 25. FORWARD BIAS SAFE OPERATING AREA

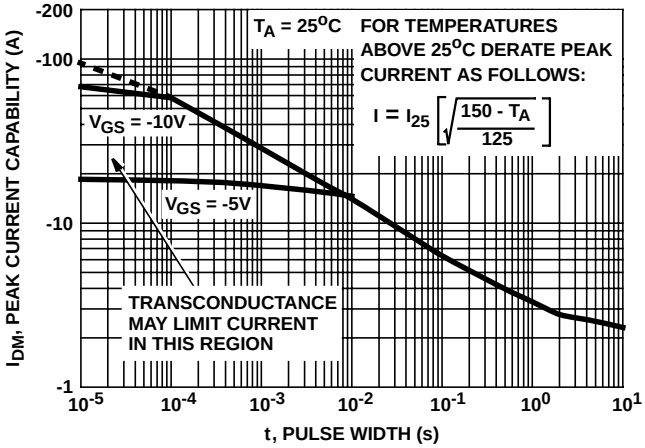
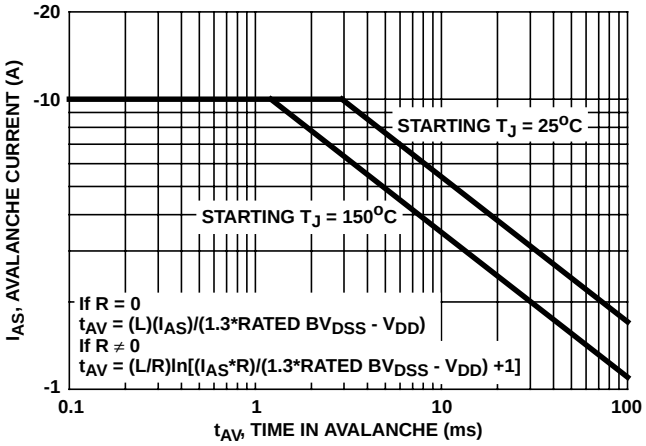



FIGURE 26. PEAK CURRENT CAPABILITY




NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 27. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

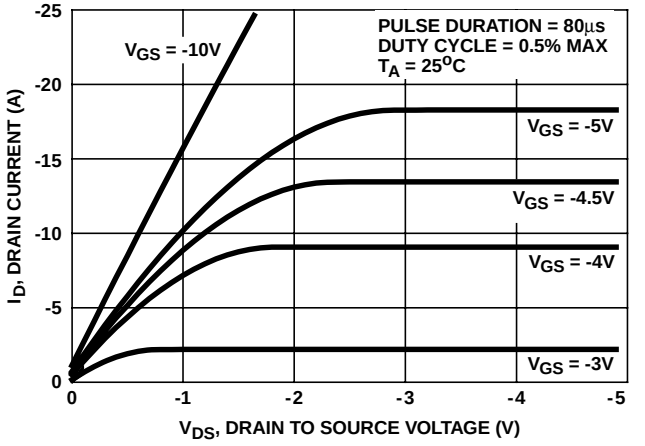



FIGURE 28. SATURATION CHARACTERISTICS

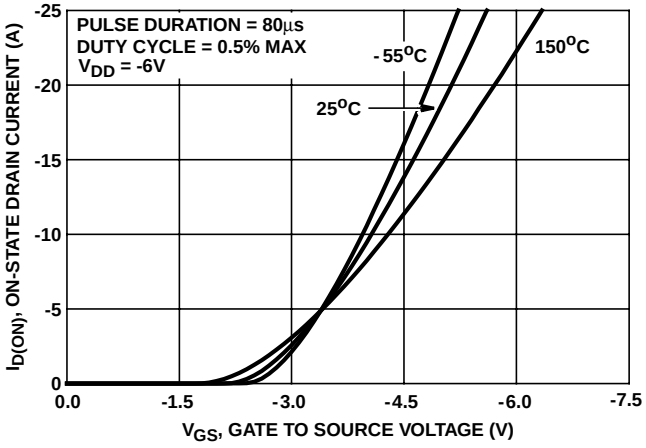



FIGURE 29. TRANSFER CHARACTERISTICS

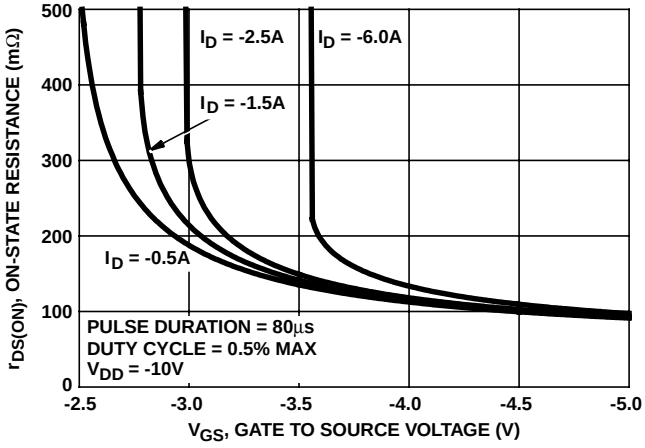



FIGURE 30. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

## Typical Performance Curves (P-Channel) (Continued)

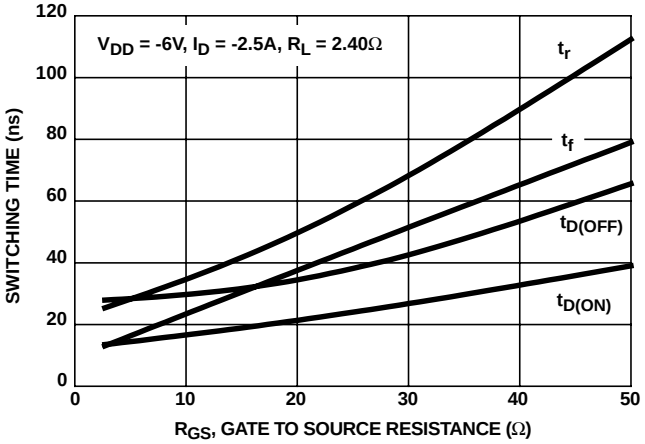



FIGURE 31. SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE

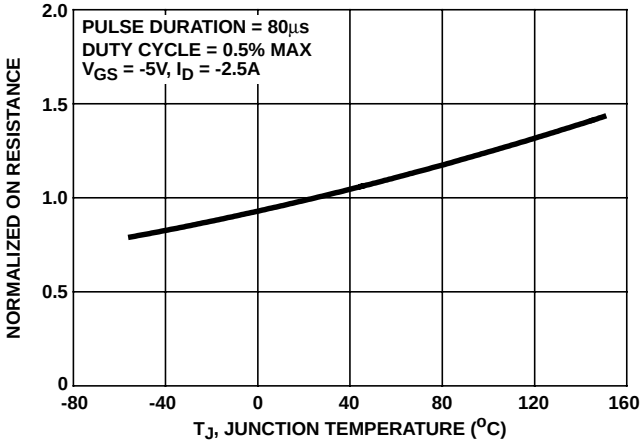



FIGURE 32. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

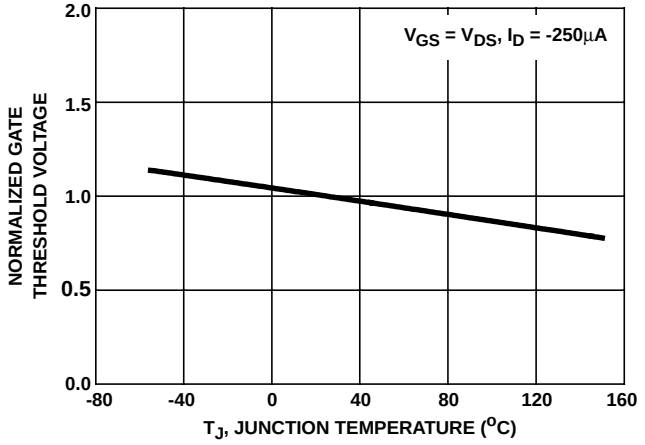



FIGURE 33. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

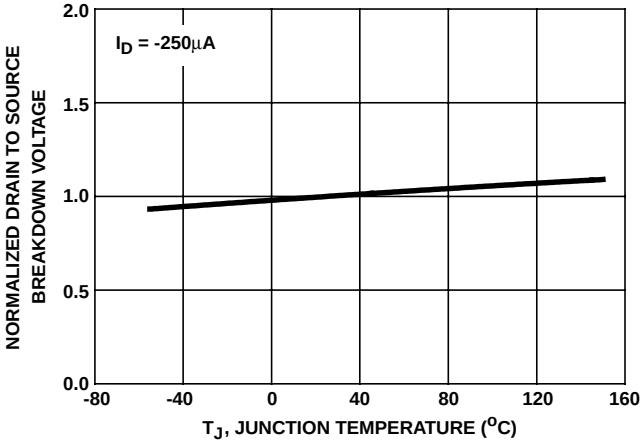



FIGURE 34. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

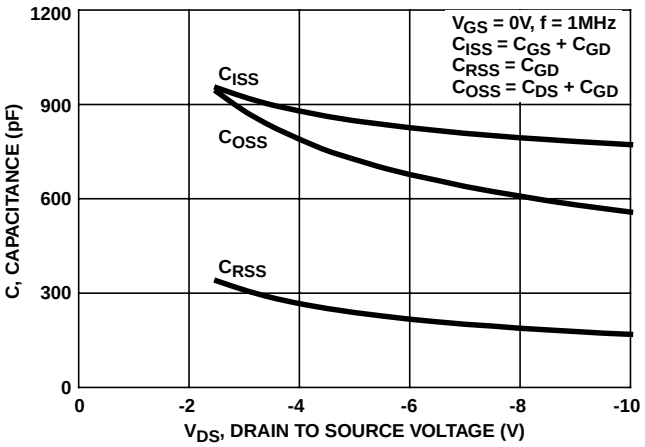
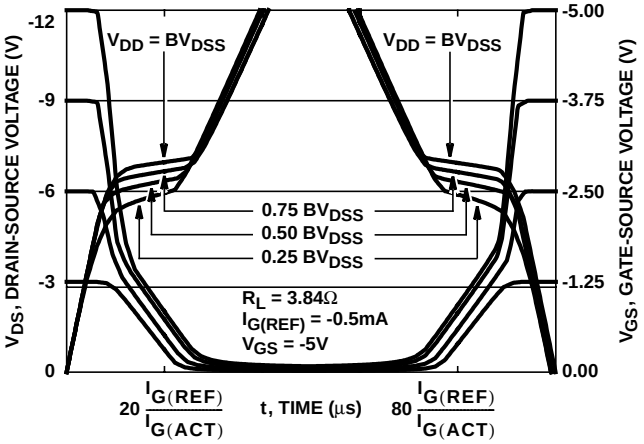



FIGURE 35. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE




NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 36. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

## Test Circuits and Waveforms (P-Channel)

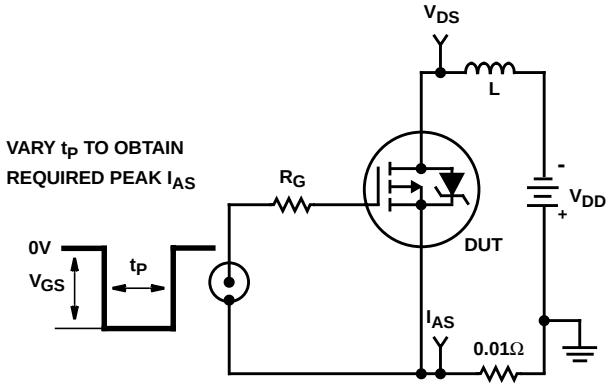



FIGURE 37. UNCLAMPED ENERGY TEST CIRCUIT

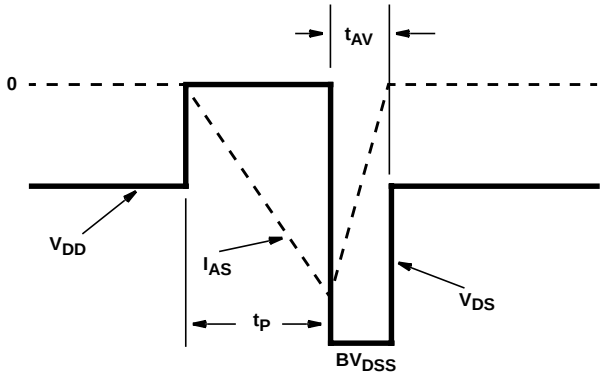



FIGURE 38. UNCLAMPED ENERGY WAVEFORMS

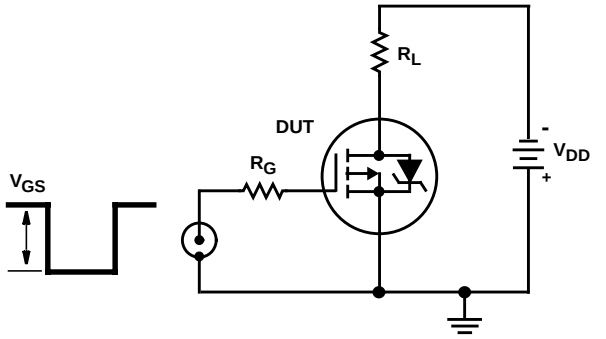



FIGURE 39. SWITCHING TIME TEST CIRCUIT

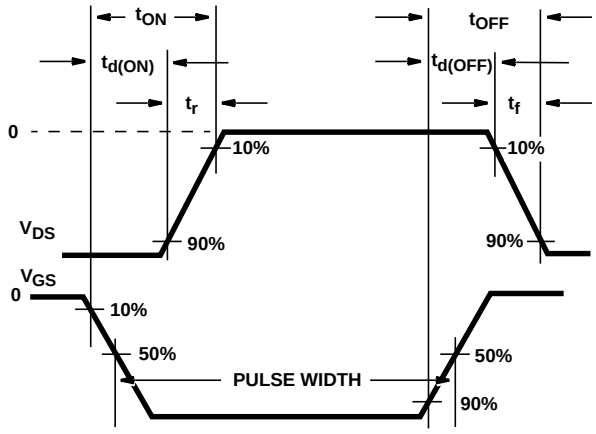



FIGURE 40. RESISTIVE SWITCHING WAVEFORMS

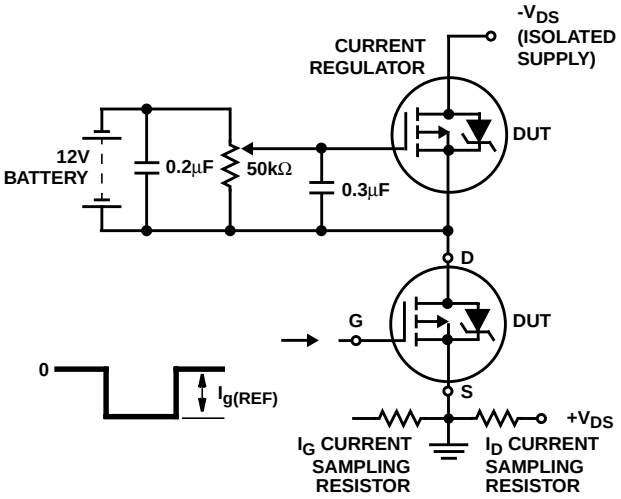



FIGURE 41. GATE CHARGE TEST CIRCUIT

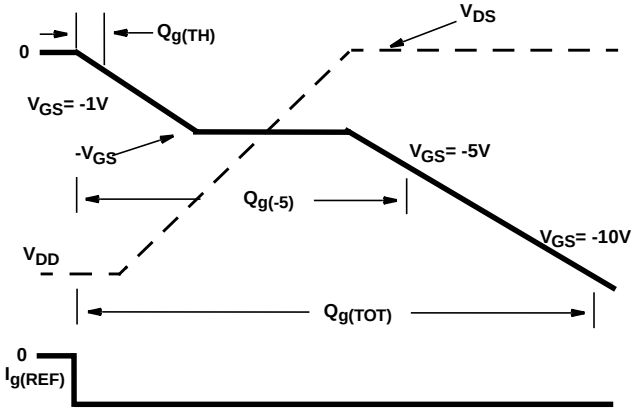



FIGURE 42. GATE CHARGE WAVEFORMS

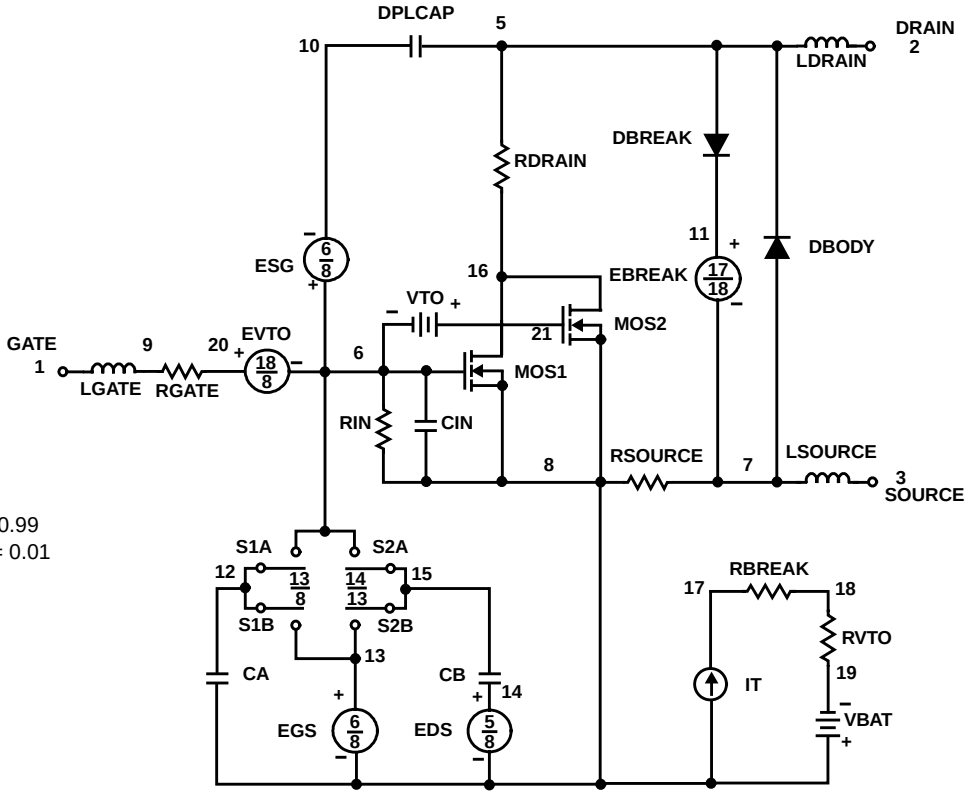
## Soldering Precautions

1. The soldering process creates a considerable thermal stress on any semiconductor component. The melting temperature of solder is higher than the maximum rated temperature of the device. The amount of time the device is heated to a high temperature should be minimized to assure device reliability. Therefore, the following precautions should always be observed in order to minimize the thermal stress to which the devices are subjected.
2. Always preheat the device.
3. The delta temperature between the preheat and soldering should always be less than $100^{o}C$. Failure to preheat the device can result in excessive thermal stress which can damage the device.
4. The maximum temperature gradient should be less than $5^{o}C$ per second when changing from preheating to soldering.
5. The peak temperature in the soldering process should be at least $30^{o}C$ higher than the melting point of the solder chosen.
6. The maximum soldering temperature and time must not exceed $260^{o}C$ for 10 seconds on the leads and case of the device.
7. After soldering is complete, the device should be allowed to cool naturally for at least three minutes, as forced cooling will increase the temperature gradient and may result in latent failure due to mechanical stress.
8. During cooling, mechanical stress or shock should be avoided.

## PSPICE Electrical Model

SUBCKT RF1K49092 2 1 3;  N-Channel Model rev 9/6/94

```
CA 12 8 9.77e-10
CB 15 14 9.19e-10
CIN  6  8  7.81e-10

DBODY  7  5  DBDMOD
DBREAK  5 11  DBKMOD
DPLCAP 10  5  DPLCAPMOD

EBREAK  11  7  17  18  14.89
EDS  14  8  5  8  1
EGS  13  8  6  8  1
ESG  6  10  6  8  1
EVTO  20  6  18  8  1

IT  8  17  1

LDRAIN  2  5  1e-9
LGATE 1  9  1.233e-9
LSOURCE  3  7  0.452e-9

MOS1  16  6  8  8  MOSMOD  M = 0.99
MOS2  16  21  8  8  MOSMOD  M = 0.01

RBREAK  17  18  RBKMOD  1
RDRAIN  5  16  RDSMOD  4.91e-3
RGATE  9  20  2.74
RIN  6  8  1e9
RSOURCE  8  7  RDSMOD  5e-3
RVTO  18  19  RVTOMOD  1

S1A  6  12  13  8  S1AMOD
S1B  13  12  13  8  S1BMOD
S2A  6  15  14  13  S2AMOD
S2B  13  15  14  13  S2BMOD

VBAT  8  19  DC  1
VTO  21  6  0.3215
```



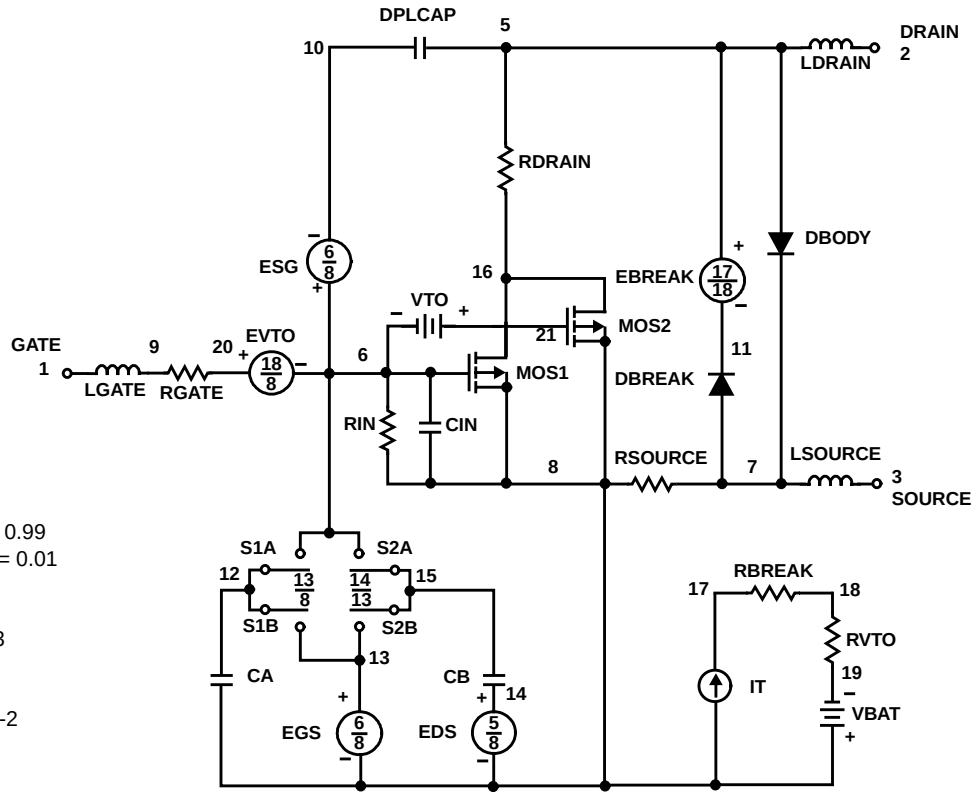

```
.MODEL DBDMOD D (IS = 7.00e-13  RS = 2.15e-2  TRS1 = 0.5e-3  TRS2 = 3.68e-6  CJO = 1.28e-9  TT = 1.8e-8)
.MODEL DBKMOD D (RS = 1.28e-1  TRS1 = 1.69e-3  TRS2 = -2.0e-6)
.MODEL DPLCAPMOD D (CJO = 0.84e-9  IS = 1e-30  N = 10)
.MODEL MOSMOD NMOS (VTO = 1.63  KP = 11.55  IS = 1e-30  N = 10  TOX = 1  L = 1u  W = 1u)
.MODEL RBKMOD RES (TC1 = 9.15e-4  TC2 = 3.13e-7)
.MODEL RDSMOD RES (TC1 = 7.00e-4  TC2 = 5.00e-6)
.MODEL RVTOMOD RES (TC1 = -2.155e-3  TC2 = -2.7e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -6.05  VOFF= -4.05)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -4.05  VOFF= -6.05)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -0.72  VOFF= 4.28)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 4.28  VOFF= -0.72)

.ENDS
```

NOTE:  For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991.

## PSPICE Electrical Model

SUBCKT RF1K49092 2 1 3 ; P-Channel Model rev 10/24/94

```
CA 12 8 8.75e-10
CB 15 14 8.65e-10
CIN 6 8 7.65e-10

DBODY 5 7 DBDMOD
DBREAK 7 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 5 11 17 18 -23.75
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 8 18 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 1.233e-9
LSOURCE 3 7 0.452e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 7.36e-3
RGATE 9 20 6.1
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 4.56e-2
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 -0.558
```




```
.MODEL DBDMOD D (IS = 3.0e-13 RS = 4.4e-2 TRS1 = 1.0e-3 TRS2 = -7.37e-6 CJO = 1.27e-9 TT = 2.2e-8)
.MODEL DBKMOD D (RS = 7.84e-2 TRS1 = -4.27e-3 TRS2 = 5.77e-5)
.MODEL DPLCAPMOD D (CJO = 2.85e-10 IS = 1e-30 N = 10)
.MODEL MOSMOD PMOS (VTO = -2.1423 KP = 9.206 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 9.61e-4 TC2 = -1.09e-6)
.MODEL RDSMOD RES (TC1 = 2.10e-3 TC2 = 6.99e-6)
.MODEL RVTOMOD RES (TC1 = -1.82e-3 TC2 = 1.47e-7)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 5.47 VOFF= 3.47)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 3.47 VOFF= 5.47)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1.05 VOFF= -3.95)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.95 VOFF= 1.05)

.ENDS
```

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991.