

## 15A, 60V, 0.150 Ohm, P-Channel Power MOSFETs

These P-Channel power MOSFETs are manufactured using the MegaFET process. This process which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA09833.

### Ordering Information

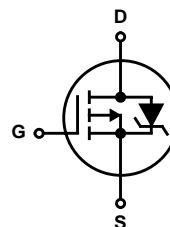
PART NUMBER	PACKAGE	BRAND
RFD15P06	TO-251AA	F15P06
RFD15P06SM	TO-252AA	F15P06
RFP15P06	TO-220AB	RFP15P06

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., RFD15P06SM9A.

### Features

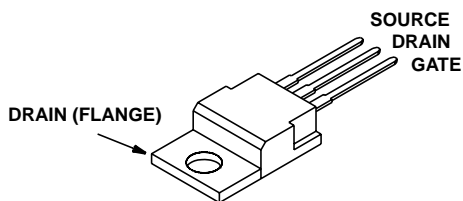
- 15A, 60V
- $r_{DS(ON)} = 0.150\Omega$
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

### Symbol

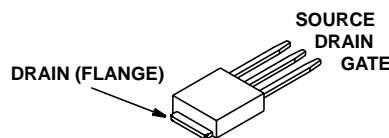


### Packaging

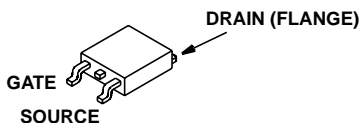
JEDEC TO-220AB



JEDEC TO-251AA



JEDEC TO-252AA



# RFD15P06, RFD15P06SM, RFP15P06

## Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ Unless Otherwise Specified

	RFD15P06, RFD15P06SM, RFP15P06	UNITS
Drain to Source Voltage (Note 1) . . . . .	$V_{DSS}$ -60	V
Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) (Note 1) . . . . .	$V_{DGR}$ -60	V
Continuous Drain Current . . . . .	$I_D$ 15	A
Pulsed Drain Current (Figure 5) (Note 3) . . . . .	$I_{DM}$ Refer to Peak Current Curve	
Gate to Source Voltage . . . . .	$V_{GS}$ $\pm 20$	V
Pulsed Avalanche Rating (Figure 6) . . . . .	$E_{AS}$ Refer to UIS Curve	
Power Dissipation . . . . .	$P_D$ 80	W
Linear Derating Factor . . . . .	0.533	W/ $^\circ\text{C}$
Operating and Storage Temperature . . . . .	$T_J, T_{STG}$ -55 to 175	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s . . . . .	$T_L$ 300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334 . . . . .	$T_{pkg}$ 260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**NOTE:**

- $T_J = 25^\circ\text{C}$  to  $150^\circ\text{C}$ .

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	-60	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	-2.0	-	-4.0	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}$	-	-	-1	$\mu\text{A}$
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, T_C = 150^\circ\text{C}$	-	-	-25	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D \approx 15\text{A}, V_{GS} = -10\text{V}$ , (Figure 9)	-	-	0.150	W
Turn-On Time	$t_{ON}$	$V_{DD} = -30\text{V}, I_D = 7.5\text{A}$ $R_L = 4.0\Omega, V_{GS} = -10\text{V}$ $R_G = 12.5\Omega$ (Figure 13)	-	-	60	ns
Turn-On Delay Time	$t_{d(ON)}$		-	16	-	ns
Rise Time	$t_r$		-	30	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	-	ns
Fall Time	$t_f$		-	20	-	ns
Turn-Off Time	$t_{OFF}$		-	-	100	ns
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0\text{V to } -20\text{V}$	-	-	150	nC
Gate Charge at -10V	$Q_{g(-10)}$	$V_{GS} = 0\text{V to } -10\text{V}$				
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0\text{V to } -2\text{V}$				
Input Capacitance	$C_{ISS}$	$V_{DS} = -25\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$ (Figure 12)	-	1150	-	pF
Output Capacitance	$C_{OSS}$		-	300	-	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	56	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	TO-220AB, TO-251AA, TO-252AA	-	-	1.875	$^\circ\text{C/W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-251AA, TO-252AA	-	-	100	$^\circ\text{C/W}$
		TO-220AB	-	-	62	$^\circ\text{C/W}$

## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	$V_{SD}$	$I_{SD} = -15\text{A}$	-	-	-1.5	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = -15\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	125	ns

**NOTES:**

- Pulsed: pulse duration  $\leq 300\text{ms}$  Max, duty cycle  $\leq 2\%$ .
- Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).

Typical Performance Curves Unless Otherwise Specified

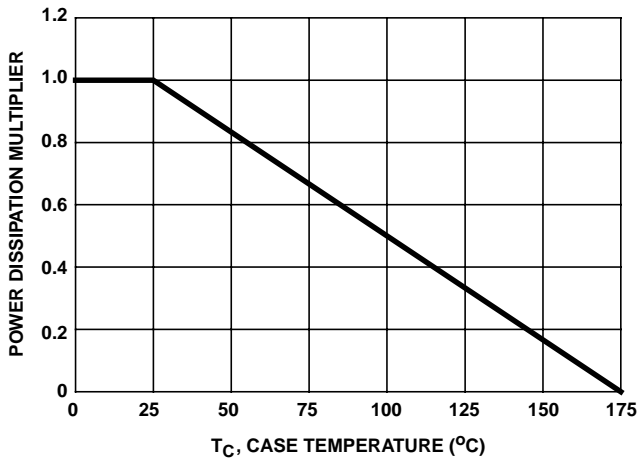


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

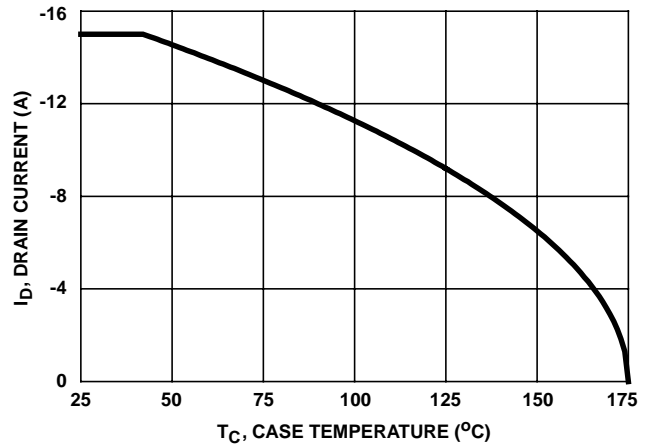


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

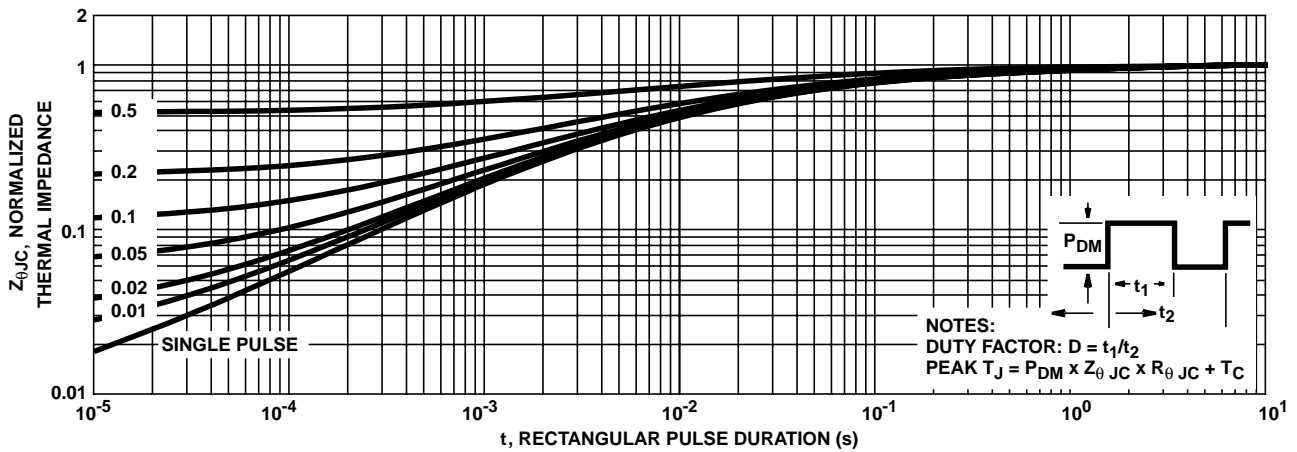


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

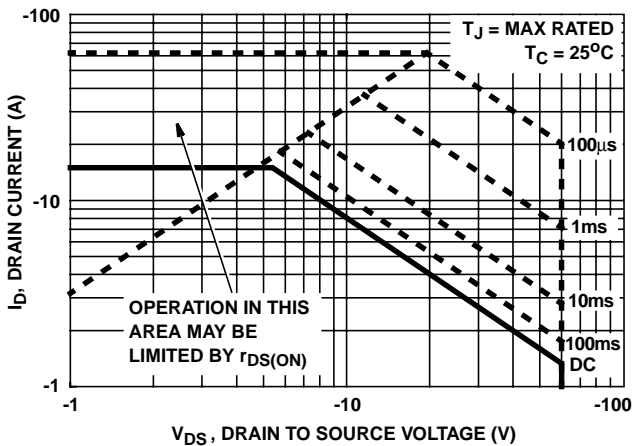


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

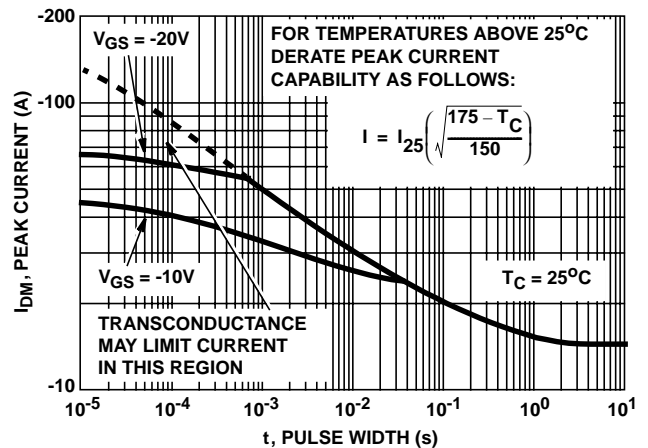
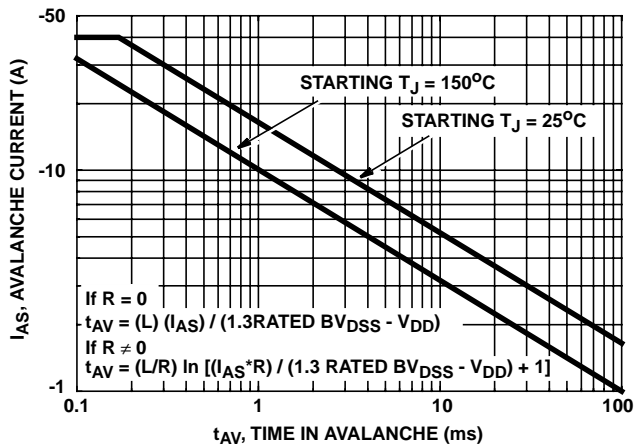


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING

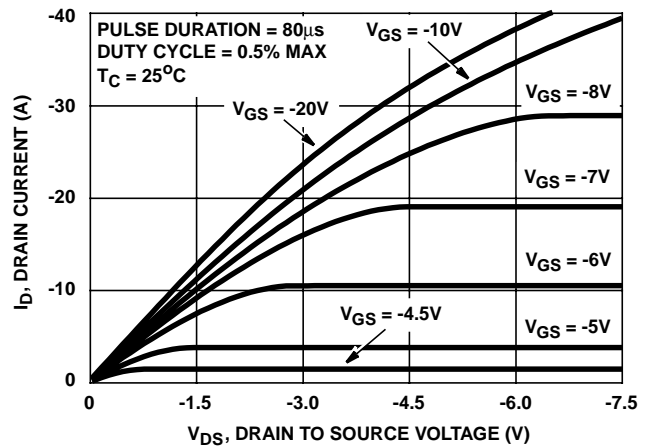


FIGURE 7. SATURATION CHARACTERISTICS

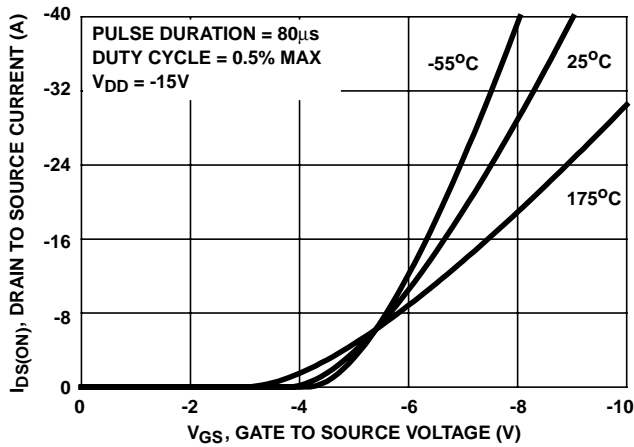


FIGURE 8. TRANSFER CHARACTERISTICS

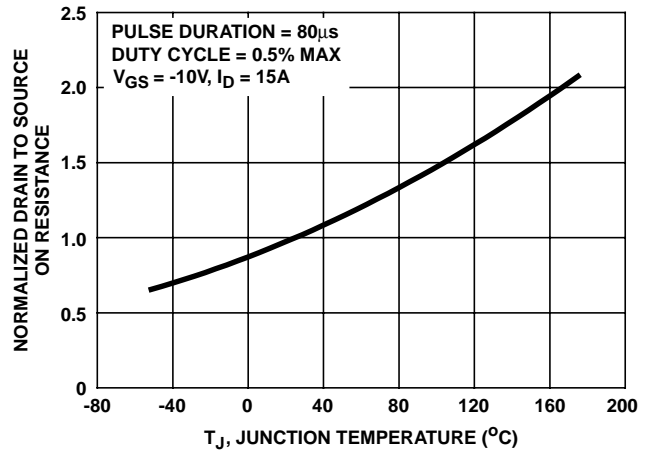


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

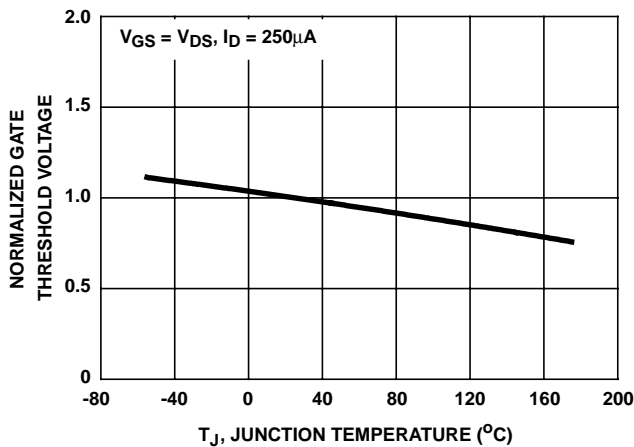


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

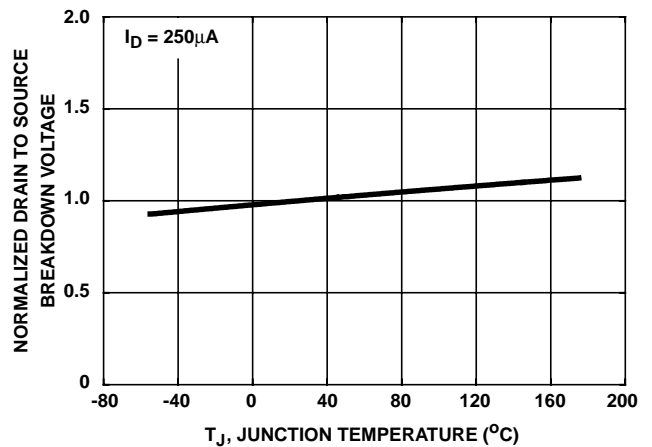


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

**Typical Performance Curves** Unless Otherwise Specified (Continued)

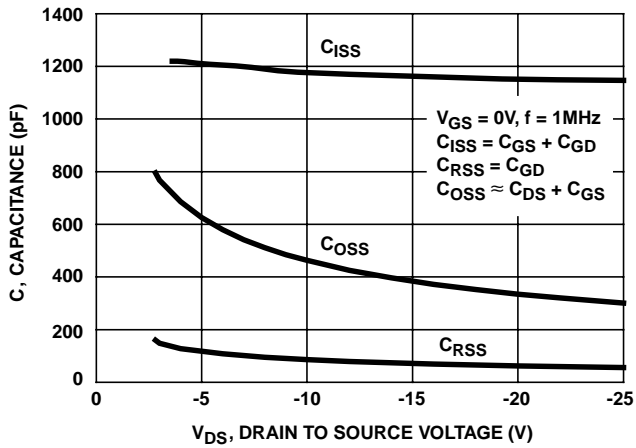
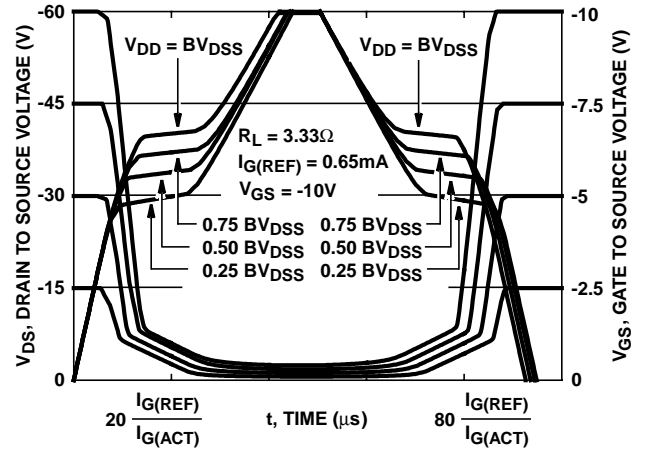


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

**Test Circuits and Waveforms**

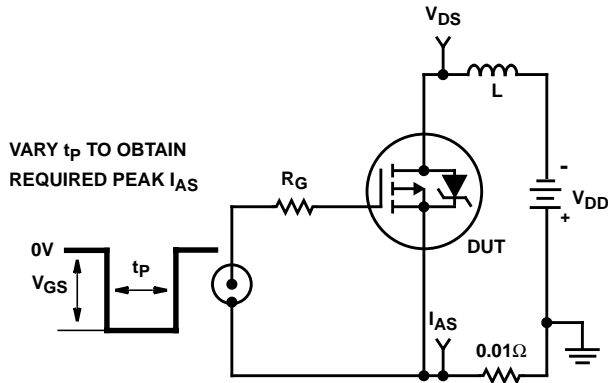


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

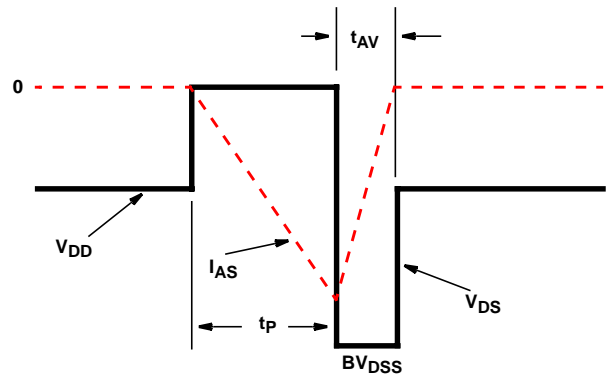


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

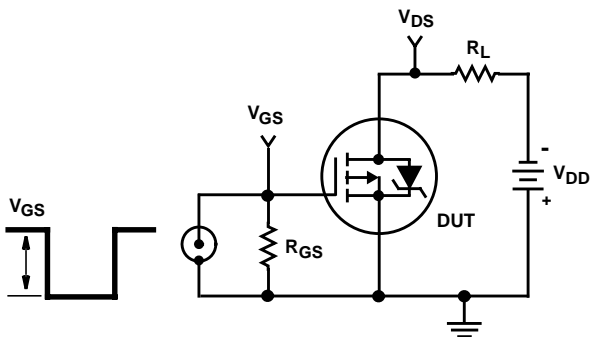


FIGURE 16. SWITCHING TIME TEST CIRCUIT

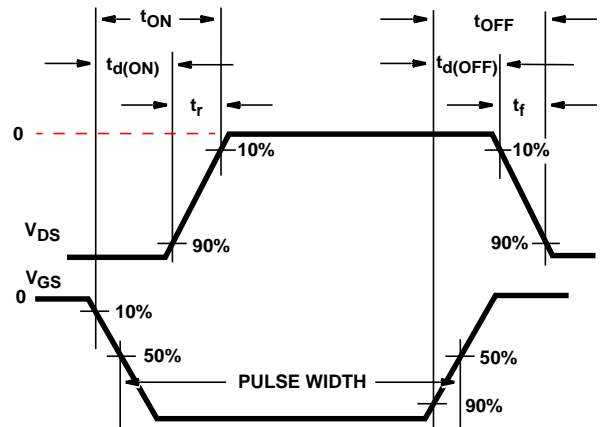


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

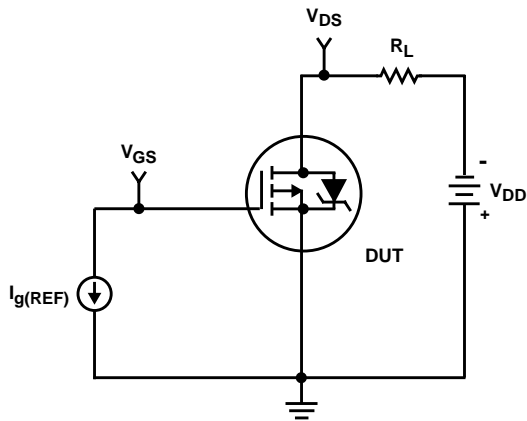


FIGURE 18. GATE CHARGE TEST CIRCUIT

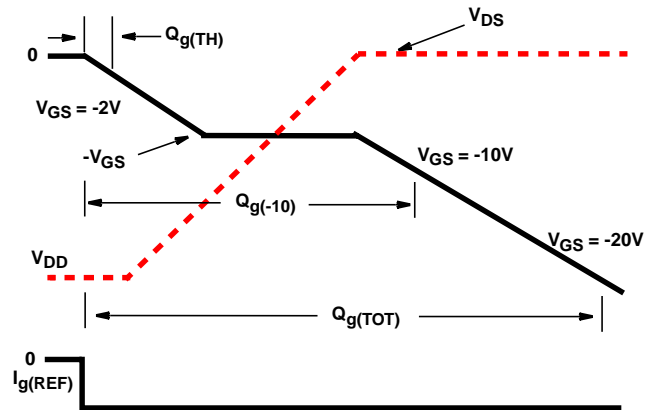


FIGURE 19. GATE CHARGE WAVEFORMS

**PSPICE Electrical Model**

.SUBCKT RFP15P06 2 1 3 REV 9/06/94

CA 12 8 1.6e-9  
 CB 15 14 1.47e-9  
 CIN 6 8 1.09e-9

DBODY 5 7 DBDMOD  
 DBREAK 7 11 DBKMOD  
 DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -73.0  
 EDS 14 8 5 8 1  
 EGS 13 8 6 8 1  
 ESG 5 10 8 6 1  
 EVTO 20 6 8 18 1

IT 8 17 1

LDRAIN 2 5 1e-9  
 LGATE 1 9 6.73e-9  
 LSOURCE 3 7 6.69e-9

MOS1 16 6 8 8 MOSMOD M = 0.99  
 MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1  
 RDRAIN 50 16 RDSMOD 63.6e-3  
 RGATE 9 20 7.37  
 RIN 6 8 1e9  
 RSCL1 5 51 RSCLMOD 1e-6  
 RSCL2 5 50 1e3  
 RSOURCE 8 7 RDSMOD 46.5e-3  
 RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD  
 S1B 13 12 13 8 S1BMOD  
 S2A 6 15 14 13 S2AMOD  
 S2B 13 15 14 13 S2BMOD

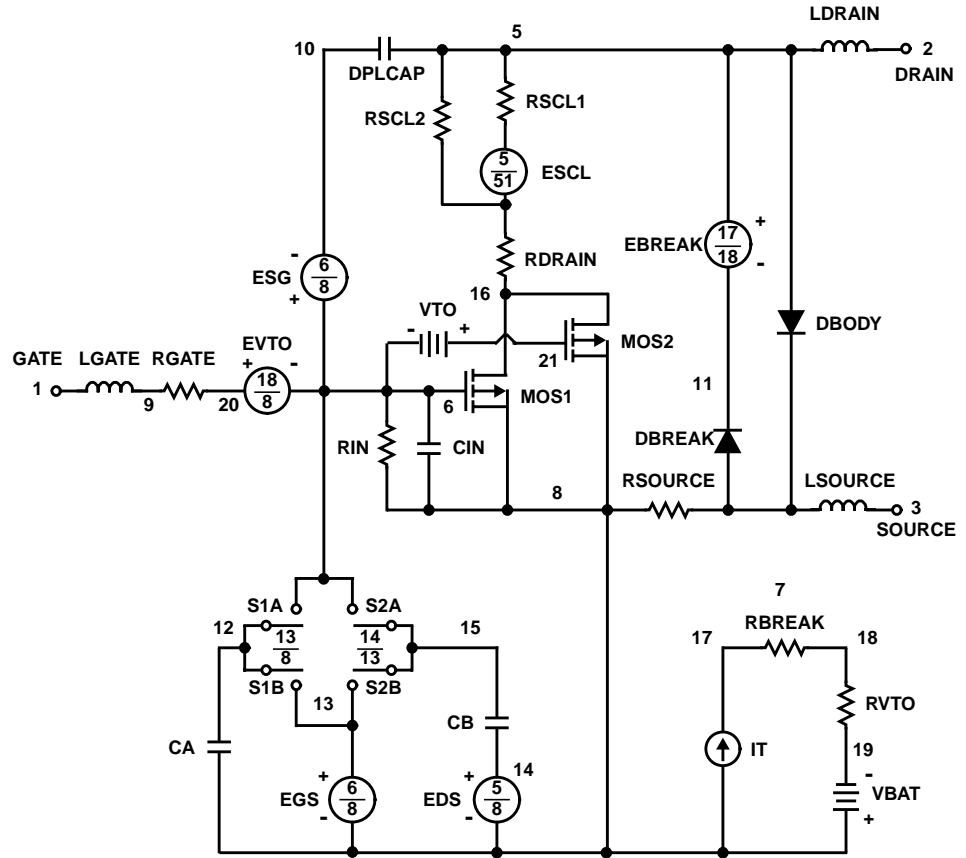
VBAT 8 19 DC 1  
 VTO 21 6 -0.65

ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51))\*1e6/35.4)}

.MODEL DBDMOD D (IS = 1.27e-13 RS = 1.62e-2 TRS1 = 1.35e-3 TRS2 = -4.33e-6 CJO = 1.25e-9 TT = 7.97e-8)  
 .MODEL DBKMOD D (RS = 2.54e-1 TRS1 = 4.54e-3 TRS2 = -1.12e-5)  
 .MODEL DPLCAPMOD D (CJO = 285e-12 IS = 1e-30 N = 10)  
 .MODEL MOSMOD PMOS (VTO = -3.78 KP = 6.97 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)  
 .MODEL RBKMOD RES (TC1 = 9.15e-4 TC2 = -4.0e-7)  
 .MODEL RDSMOD RES (TC1 = 5.47e-3 TC2 = 1.37e-5)  
 .MODEL RSCLMOD RES (TC1 = 1.9e-3 TC2 = -7.5e-6)  
 .MODEL RVTOMOD RES (TC1 = -3.71e-3 TC2 = -2.41e-6)  
 .MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 3.65 VOFF = 1.65)  
 .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1.65 VOFF = 3.65)  
 .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.60 VOFF = -4.40)  
 .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.40 VOFF = 0.60)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

*Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

### **Sales Office Headquarters**

#### **NORTH AMERICA**

Intersil Corporation  
P. O. Box 883, Mail Stop 53-204  
Melbourne, FL 32902  
TEL: (407) 724-7000  
FAX: (407) 724-7240

#### **EUROPE**

Intersil SA  
Mercure Center  
100, Rue de la Fusee  
1130 Brussels, Belgium  
TEL: (32) 2.724.2111  
FAX: (32) 2.724.22.05

#### **ASIA**

Intersil (Taiwan) Ltd.  
7F-6, No. 101 Fu Hsing North Road  
Taipei, Taiwan  
Republic of China  
TEL: (886) 2 2716 9310  
FAX: (886) 2 2715 3029