HI5780

10-Bit, 80 MSPS, High Speed, Low Power D/A Converter

August 1997

Features

- **Throughput Rate . . . . . 80 MSPS**
- **Low Power 150mW**
- **Differential Linearity Error . . . . . ±0.5 LSB**
- **TTL/CMOS Compatible Inputs**
- **Built in Bandgap Voltage Reference**
- **Power Down and Blanking Control Pins**
- **Direct Replacement for Sony CXD2306**

Applications

- **Wireless Communications**
- **Direct Digital Frequency Synthesis**
- **Signal Reconstruction**
- **Test Equipment**
- **High Resolution Imaging and Graphics Systems**
- **Arbitrary Waveform Generators**

Description

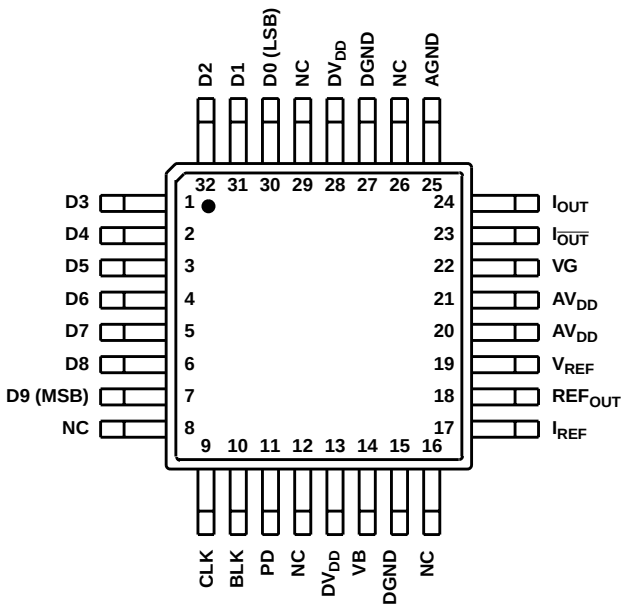
The HI5780 is a 10-bit, 80 MSPS, high speed, low power CMOS D/A converter. The converter incorporates a 10-bit input data register with current outputs. The HI5780 includes a power down feature that reduces power consumption and a blanking control. The on-chip bandgap reference can be used to set the output current range of the D/A.

Ordering Information

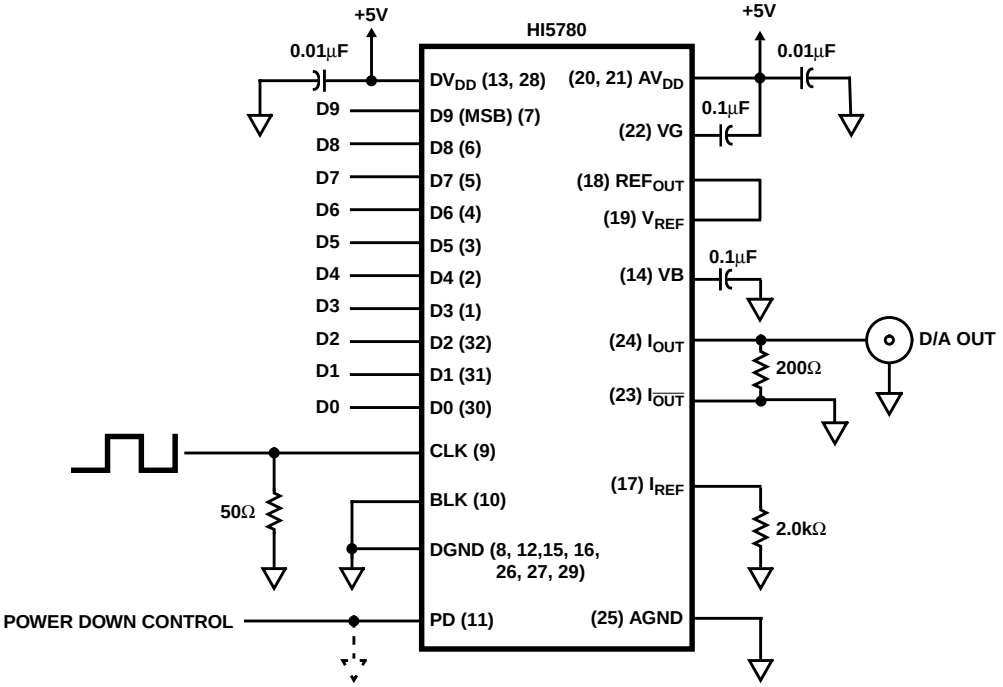
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI5780JCQ	-20 to 75	32 Ld MQFP	Q32.7x7-S
HI5780-EV	25	Evaluation Kit	

Pinout

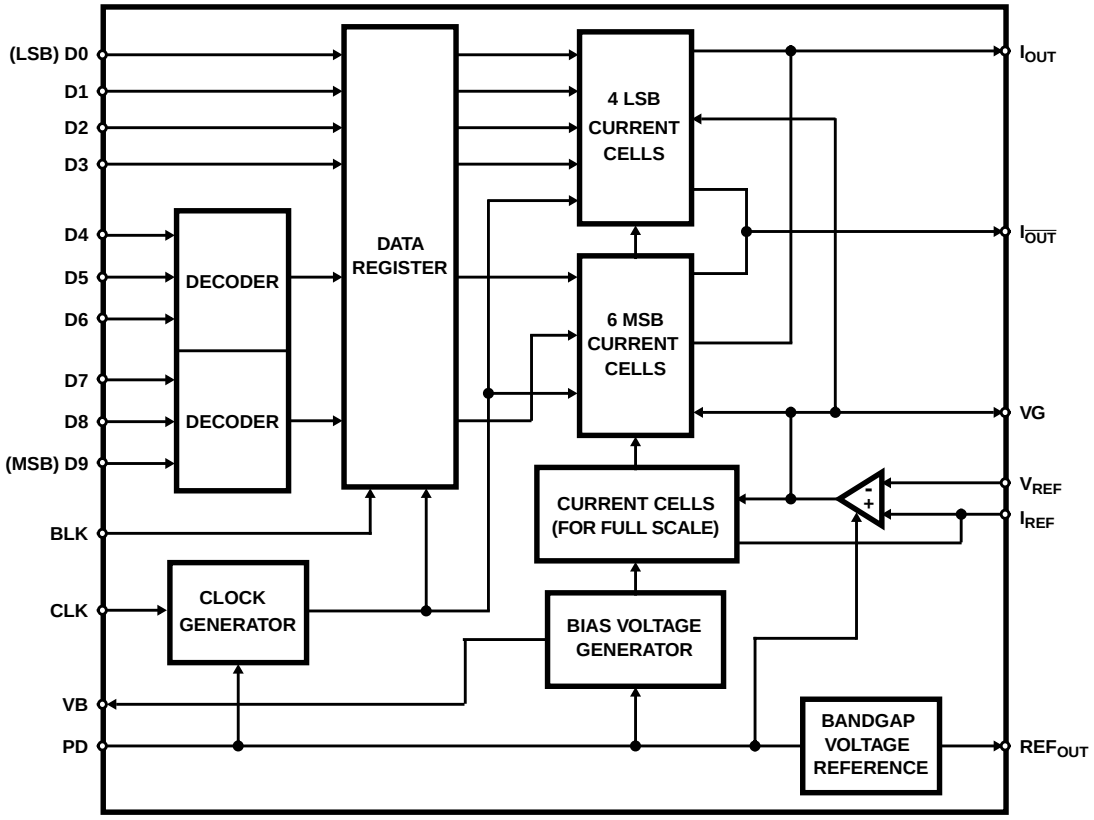
HI5780
(MQFP)



Typical Application Circuit



Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage V_{DD} to DGND . . . . . +7.0V
Digital Input Voltages (D9-D0, CLK, BLANK, PD) . . . . V_{DD} to -0.5V
Internal Reference Output Current . . . . . ±2.5mA
Reference Input Voltage Range (V_{REF}) . . . . . V_{DD} to -0.5 V
Analog Output Current (I_{OUT}) 15mA

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
MQFP Package 122
Maximum Junction Temperature (Plastic Package)
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C
(MQFP - Lead Tips Only)

Operating Conditions

Temperature Range, HI5780BIx . . . . . -20^{o}C to 75^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

AV_{DD}, DV_{DD} = 5.00V, V_{REF} = 2.0V, f_{CLK} = 80 MSPS, R_{LOAD} = 200Ω, R_{REF} = 3.3kΩ, T_A = 25^{o}C

PARAMETER	TEST CONDITIONS	HI5780JCQ			UNITS
		MIN	TYP	MAX	
SYSTEM PERFORMANCE					
Resolution		10	-	-	Bits
Integral Linearity Error, INL	(Notes 4, 5) ("Best Fit" Straight Line)	-2.0	1.25	2.0	LSB
Differential Linearity Error, DNL	(Notes 4, 5)	-0.5	0.25	0.5	LSB
Offset Error, I_{OS}	(Notes 4, 5)	-	-	5	µA
Full Scale Output Current, I_{FS}	(Note 4)	9.0	9.6	10	mA
Full Scale Drift Coefficient, I_{DRIFT}	(Note 2)	-	0.26	-	mV/^{o}C
Output Voltage Compliance Range	(Note 3), 10-Bit Accuracy	1.8	1.92	2.0	V
DYNAMIC CHARACTERISTICS					
Throughput Rate	(Note 3)	80.0	-	-	MSPS
Output Voltage Full Scale Step Settling Time, $t_{SETT\ FS}$	To ±0.5 LSB Error Band R_L = 75Ω, 10-Bit Accuracy (Note 3)	-	6.0	-	ns
Singlet Glitch Area, GE (Peak)	R_{LOAD} = 75Ω, V_{OUT} = 1.0V_{P-P} (Note 3)	-	40	-	pV-s
Differential Gain, DG	(Note 4)	-	2.5	-	%
Differential Phase, DP	(Note 4)	-	1.3	-	Degrees
Spurious Free Dynamic Range, SFDR to Nyquist	f_{CLK} = 40 MSPS, f_{OUT} = 2.02MHz, 20MHz Span (Note 3)	-	48.5	-	dBc
	f_{CLK} = 80 MSPS, f_{OUT} = 2.02MHz, 40MHz Span (Note 3)	-	47.5	-	dBc
	f_{CLK} = 40 MSPS, f_{OUT} = 10MHz, 20MHz Span (Note 3)	-	40.75	-	dBc
	f_{CLK} = 80 MSPS, f_{OUT} = 20MHz, 40MHz Span (Note 3)	-	38.5	-	dBc
Spurious Free Dynamic Range, SFDR Within a Window	f_{CLK} = 40 MSPS, f_{OUT} = 2.02MHz, 2MHz Span (Note 3)	-	75.0	-	dBc
	f_{CLK} = 80 MSPS, f_{OUT} = 2.02MHz, 2MHz Span (Note 3)	-	73.5	-	dBc
	f_{CLK} = 40 MSPS, f_{OUT} = 10MHz, 2MHz Span (Note 3)	-	56.5	-	dBc
	f_{CLK} = 80 MSPS, f_{OUT} = 20MHz, 2MHz Span (Note 3)	-	49.0	-	dBc
REFERENCE					
Internal Reference Voltage, REF_{OUT}	(Notes 4, 5)	1.0	1.25	1.3	V
Internal Reference Voltage Drift	(Note 3)	-	0.34	-	mV/^{o}C
Reference Input Voltage Range, V_{REF}	(Note 3)	0.5	-	2.0	V

Electrical Specifications AV_{DD}, DV_{DD} = 5.00V, V_{REF} = 2.0V, f_{CLK} = 80 MSPS, R_{LOAD} = 200Ω, R_{REF} = 3.3kΩ, T_A = 25°C **(Continued)**

PARAMETER	TEST CONDITIONS	HI5780JCQ			UNITS
		MIN	TYP	MAX	
DIGITAL INPUTS (D9-D0, CLK, BLK, PD)					
Input Logic High Voltage, V_{IH}	(Note 5)	2.15	-	-	V
Input Logic Low Voltage, V_{IL}	(Note 5)	-	-	0.85	V
Input Logic Current, I_{IH}	(Note 5)	-	-	5	µA
Input Logic Current, I_{IL}	(Note 5)	-5	-	-	µA
Digital Input Capacitance, C_{IN}	(Note 3)	-	3.0	-	pF
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	(See Figure 1, Note 3)	5.0	3.0	-	ns
Data Hold Time, t_{HLD}	(See Figure 1, Note 3)	1.0	0	-	ns
Propagation Delay Time, t_{PD}	(See Figure 1, Note 3)	-	8.0	-	ns
CLK Pulse Width, t_{PW1}, t_{PW2}	(See Figure 1, Note 3)	6.25	-	-	ns
POWER SUPPLY CHARACTERISTICS					
IV_{DD}	(Notes 4, 5)	-	20	30	mA
Power Dissipation	(Note 5)	-	100	150	mW
Sleep Mode Power Consumption	PD = 1 (Note 4)	-	1.25	-	mW

NOTES:

2. R_{LOAD} is connected to I_{OUT} (pin 24) and R_{REF} is connected to I_{REF} (pin 17).
3. Parameter guaranteed by design or characterization and not production tested.
4. Typical values are test results at T_A = 25°C.
5. All devices are 100% tested at 25°C.

Timing Diagrams

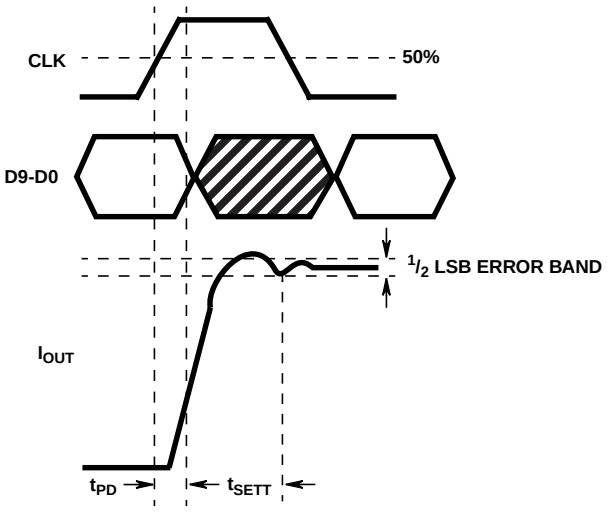


FIGURE 1. FULL SCALE SETTLING TIME DIAGRAM

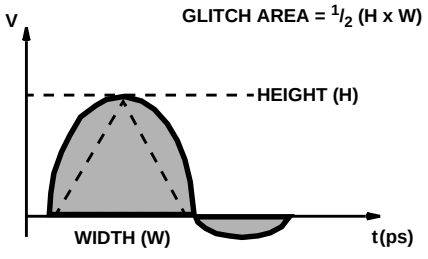


FIGURE 2. PEAK GLITCH AREA (SINGLET) MEASUREMENT METHOD

Timing Diagrams (Continued)

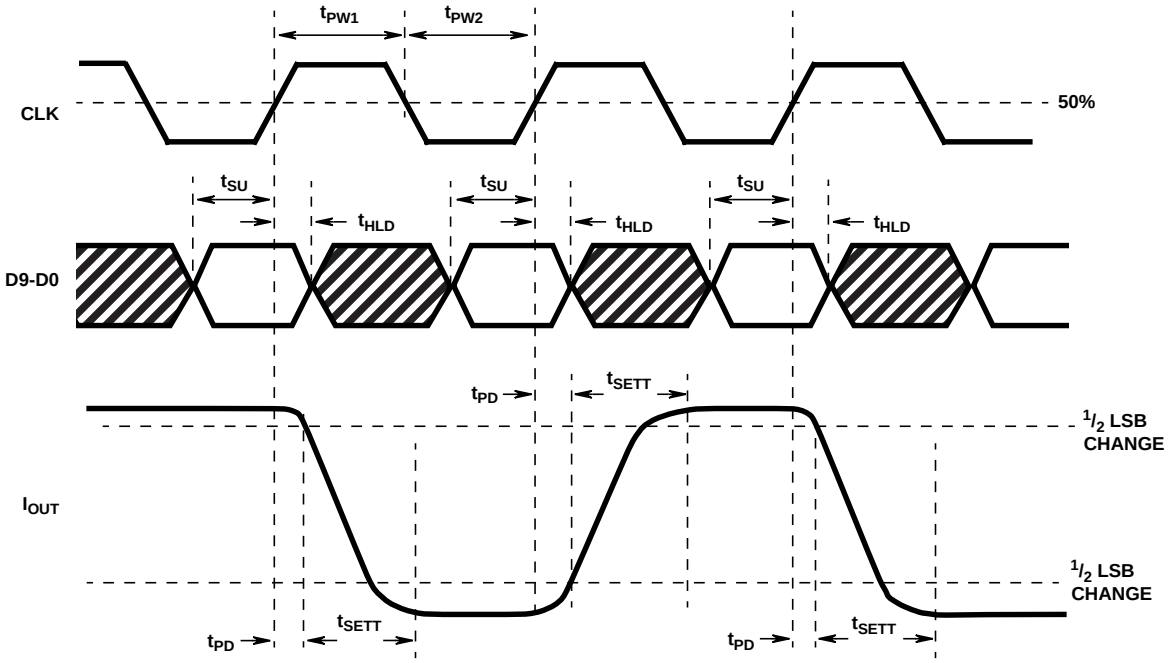


FIGURE 3. PROPAGATION DELAY, SETUP TIME AND MINIMUM PULSE WIDTH DIAGRAM

Pin Descriptions

PIN	PIN NAME	DESCRIPTION
1-7, 30-32	D0 (LSB) thru D9 (MSB)	Digital Data Bit 0, the least significant bit thru digital data Bit 9, the most significant bit.
9	CLK	Data Clock Pin 100kHz to 80MHz.
13, 28	DV_{DD}	Digital Logic Supply +5V.
15, 27	DGND	Digital Ground.
20, 21	AV_{DD}	Analog Supply +5V.
23	BLK	Output Blanking pin. When set (‘1’) this pin zeros the I_{OUT} pin.
25	AGND	Analog Ground Supply Current Return pin.
11	PD	Power Down Mode pin. This pin when set (‘1’) places the HI5780 in lower power mode and zeros the output. Power consumption is reduced.
24	I_{OUT}	Current Output pin.
23	I_{OUT}	Complementary Current Output pin.
18	REF_{OUT}	Bandgap Reference Voltage Output.
17	I_{REF}	Reference Current setting resistor connected from here to Ground.
19	V_{REF}	Reference Voltage Input pin.
14	VB	Bias Voltage Generator Bypass Capacitor connected from here to Ground.
22	VG	Reference Amplifier Bypass Capacitor connected from here to AV_{DD}.

Typical Performance Curves

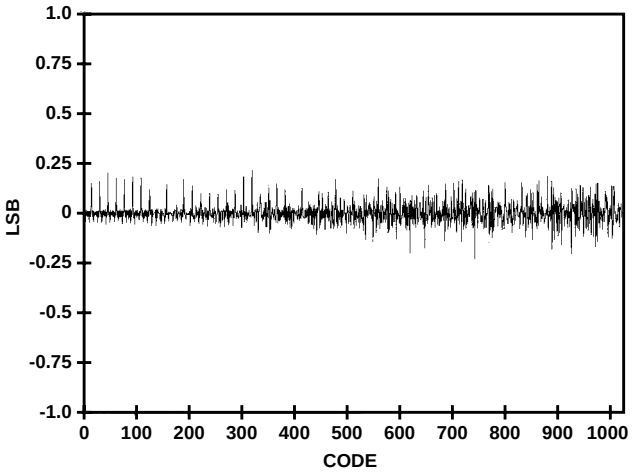


FIGURE 4. DIFFERENTIAL LINEARITY

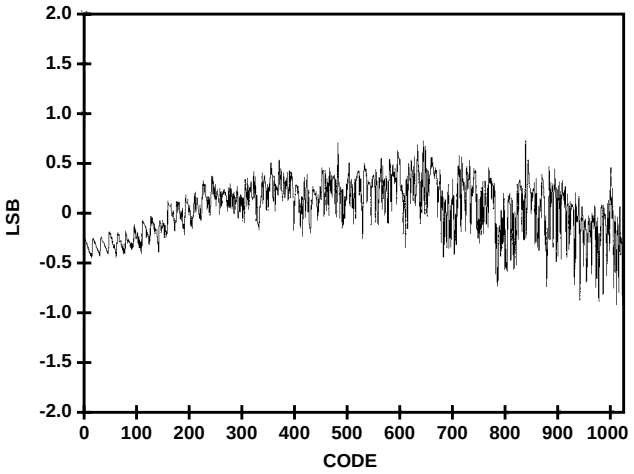


FIGURE 5. INTEGRAL LINEARITY (BEST FIT - STRAIGHT LINE)

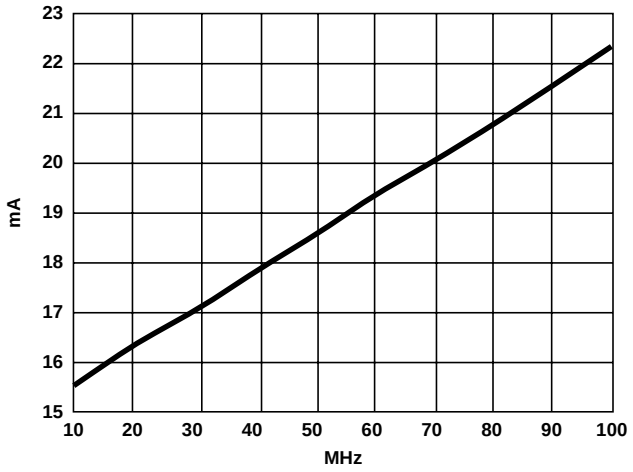


FIGURE 6. POWER SUPPLY CURRENT vs CLOCK FREQUENCY

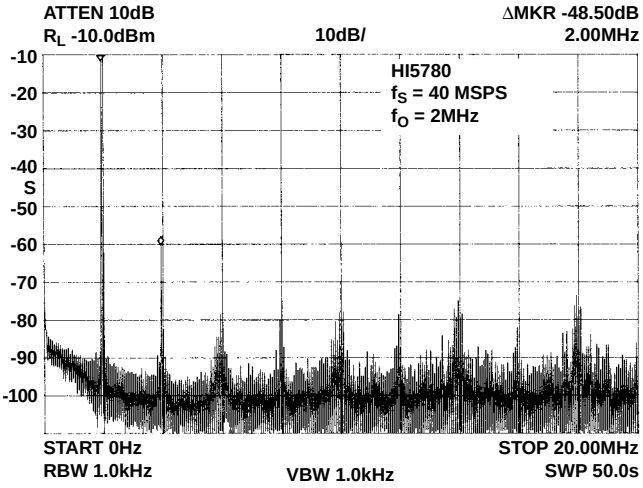


FIGURE 7. SPURIOUS FREE DYNAMIC RANGE TO NYQUIST

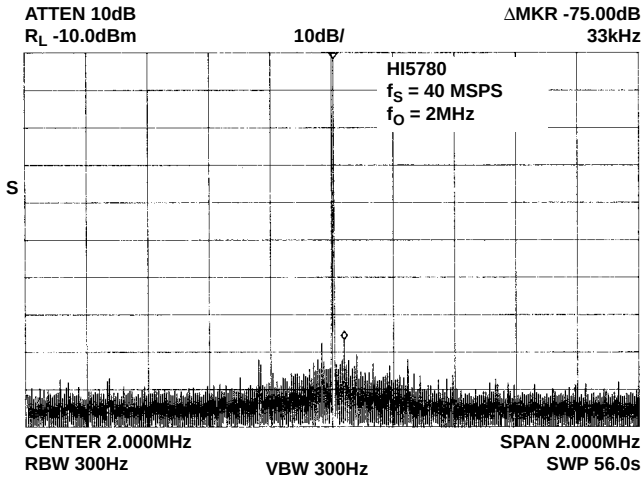


FIGURE 8. SPURIOUS FREE DYNAMIC RANGE WITHIN A WINDOW

Detailed Description

The HI5780 is a 10-bit, current out D/A converter. The DAC can convert at 80 MSPS and runs on +5V supplies. The HI5780 achieves its low power and high speed performance from an advanced CMOS process. The HI5780 consumes 150mW (Maximum) and has a power down mode that only consumes 1.25mW when in sleep mode. The HI5780 is an excellent converter to be used for communications applications and high performance video systems.

Digital Inputs

The HI5780 is a TTL/CMOS-compatible D/A. Data is latched by a 10-bit latch. Once latched data inputs D0 (LSB) thru D9 (MSB) are decoded to the internal current cells; the internal latch and switching current source controls are implemented in CMOS technology to maintain high switching speeds and low power consumption.

Clocks and Termination

The internal 10-bit register is updated on the rising edge of the clock. Since the HI5780 clock rate can run to 80MHz, to minimize reflections and clock noise into the part, proper termination should be used. In PCB layout clock runs should be kept short and have a minimum of loads. To guarantee consistent results from board to board, controlled impedance PCBs should be used with a characteristic line impedance, Z_O, of 50Ω.

To terminate the clock line a shunt terminator to ground is the most effective type at a 80 MSPS clock rate. A typical value for termination can be determined by the equation:

$$R_T = Z_O,$$

for the termination resistor. For a controlled impedance board with a Z_O of 50Ω, the R_T = 50Ω. Shunt termination is best used at the receiving end of the transmission line or as close to the HI5780 CLK pin as possible.

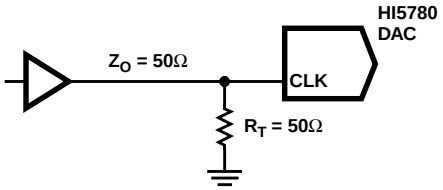


FIGURE 9. AC TERMINATION OF THE HI5780 CLOCK LINE

Rise and Fall times and propagation delay of the line will be affected by the Shunt Terminator. The terminator can be connected to DGND.

Noise Reduction

To reduce power supply noise, separate analog and digital power supplies should be used with 0.1µF and 0.01µF ceramic capacitors placed as close to the body of the HI5780 as possible on the analog (AV_{DD}) and digital (DV_{DD}) supplies. The analog and digital ground returns should be connected together back at the device to ensure proper operation on power up.

Reference

The internal reference in the HI5780 is a 1.25V (typical) bandgap voltage reference. The internal reference is buffered by an amplifier to provide adequate drive for the current cells. Reference Out (REF_{OUT}) is connected to the V_{REF} pin. The Full Scale Output Current is controlled by the resistor connected to I_{REF}. The full scale output voltage, is set by the following equation:

$$V_{OUT}(\text{Full Scale}) = V_{REF} \times 16(R_{LOAD}/R_{REF}).$$

Applications

Voltage Conversion of the Output

To convert the output current of the D/A converter to a voltage, an amplifier should be used as shown in Figure 5. The DAC needs a 50Ω termination resistor on the I_{OUT} pin to ensure proper settling. The HFA1110 has an internal feedback resistor to compensate for high frequency operation.

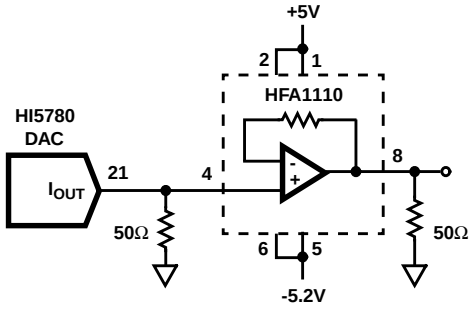


FIGURE 10. HIGH SPEED CURRENT TO VOLTAGE CONVERSION

Definition of Specifications

Integral Linearity Error, INL, is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Differential Linearity Error, DNL, is the measure of the step size output deviation from code to code. Ideally the step size should be 1 LSB. A DNL specification of 1 LSB or less guarantees monotonicity.

Output Voltage Full Scale Settling Time, is the time required from the 50% point on the clock input for a full scale step to settle within an $^1/_2$ LSB error band.

Glitch Area, GE, is the switching transient appearing on the output during a code transition. It is measured as the area under the curve and expressed as a Volt-Time specification.

Differential Gain, ΔA_V, is the gain error from an ideal sine wave with a normalized amplitude.

Differential Phase, $\Delta\Phi$, is the phase error from and ideal sine wave.

Spurious Free Dynamic Range, SFDR, is the amplitude difference from a fundamental to the largest harmonically or non-harmonically related spur. A sine wave is loaded into the D/A and the output filtered at $^1/_2$ the clock frequency to eliminate noise from clocking alias terms.

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