

## Radiation Hardened, Ultra High Speed Current Feedback Amplifier with Offset Adjust

August 1996

### Features

- Electrically Screened to SMD 5962F9675601VPA
- MIL-PRF-38535 Class V Compliant
- Low Distortion (HD3, 30MHz) . . . . . -84dBc (Typ)
- Wide -3dB Bandwidth . . . . . 850MHz (Typ)
- Very High Slew Rate . . . . . 2300V/ $\mu$ s (Typ)
- Fast Settling (0.1%) . . . . . 11ns (Typ)
- Excellent Gain Flatness (to 50MHz) . . . . . 0.05dB (Typ)
- High Output Current . . . . . 65mA (Typ)
- Fast Overdrive Recovery . . . . . <10ns (Typ)
- Total Gamma Dose . . . . . 300K RAD (Si)
- Latch Up . . . . . None (DI Technology)

### Applications

- Video Switching and Routing
- Pulse and Video Amplifiers
- Wideband Amplifiers
- RF/IF Signal Processing
- Flash A/D Driver
- Imaging Systems

### Description

The HS-1120RH is a radiation hardened, high speed, wideband, fast settling current feedback amplifier. These devices are QML approved and are processed and screened in full compliance with MIL-PRF-38535. Built with Intersil' proprietary, complementary bipolar UHF-1 (DI bonded wafer) process, it is the fastest monolithic amplifier available from any semiconductor manufacturer.

The HS-1120RH's wide bandwidth, fast settling characteristic, and low output impedance, make this amplifier ideal for driving fast A/D converters. Additionally, it offers offset voltage nulling capabilities as described in the "Offset Adjustment" section of this datasheet.

Component and composite video systems will also benefit from this amplifier's performance, as indicated by the excellent gain flatness, and 0.03%/0.05 Degree Differential Gain/Phase specifications ( $R_L = 75\Omega$ ).

Detailed electrical specifications are contained in SMD 5962F9675601VPA, available on the Intersil Website or AnswerFAX systems (document #967560)

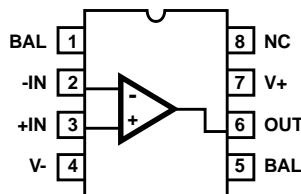
A Cross Reference Table is available on the Intersil Website for conversion of Intersil Part Numbers to SMDs. The address is ([http://www.intersil.com/datasheets/smd/smd\\_xref.html](http://www.intersil.com/datasheets/smd/smd_xref.html)). SMD numbers must be used to order Radiation Hardened Products.

### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
5962F9675601VPA	-55 to 125	8 Ld CERDIP	GDIP1-T8
HFA1100IJ (Sample)	-40 to 85	8 Ld CERDIP	F8.3A
HFA11XXEVAL	Evaluation Board		

### Pinout

HS-1120RH  
MIL-STD-1835, GDIP1-T8  
(CERDIP)  
TOP VIEW



## Application Information

### Optimum Feedback Resistor

The enclosed plots of inverting and non-inverting frequency response illustrate the performance of the HS-1120RH in various gains. Although the bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and  $R_F$ . All current feedback amplifiers require a feedback resistor, even for unity gain applications, and  $R_F$ , in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to  $R_F$ . The HS-1120RH design is optimized for a 510Ω  $R_F$  at a gain of +1. Decreasing  $R_F$  in a unity gain application decreases stability, resulting in excessive peaking and overshoot. At higher gains the amplifier is more stable, so  $R_F$  can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended  $R_F$  values for various gains, and the expected bandwidth.

GAIN ( $A_{CL}$ )	$R_F$ (Ω)	BANDWIDTH (MHz)
-1	430	580
+1	510	850
+2	360	670
+5	150	520
+10	180	240
+19	270	125

### PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value (0.1μF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to -IN, and connections to -IN should be kept as short as possible.

An example of a good high frequency layout is the Evaluation Board shown in Figure 2.

## Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor ( $R_S$ ) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the  $R_S$  and  $C_L$  combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

$R_S$  and  $C_L$  form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 850MHz. By decreasing  $R_S$  as  $C_L$  increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. Even so, bandwidth does decrease as you move to the right along the curve. For example, at  $A_V = +1$ ,  $R_S = 50\Omega$ ,  $C_L = 30pF$ , the overall bandwidth is limited to 300MHz, and bandwidth drops to 100MHz at  $A_V = +1$ ,  $R_S = 5\Omega$ ,  $C_L = 340pF$ .

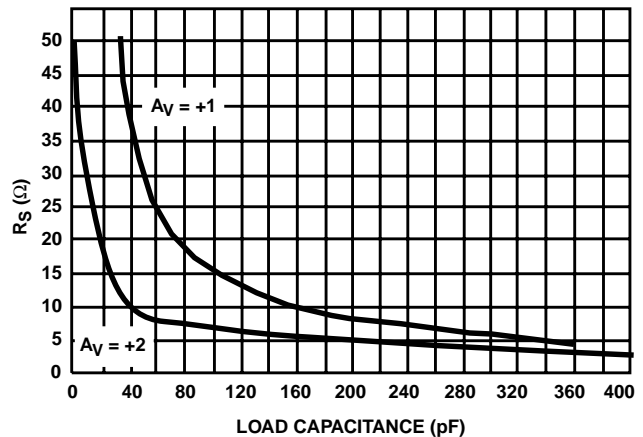


FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

## Evaluation Board

The performance of the HS-1120RH may be evaluated using the HFA11XXEVAL Evaluation Board.

The layout and schematic of the board are shown in Figure 2. To order evaluation boards, please contact your local sales office.

## Offset Adjustment

The output offset voltage of the HS-1120RH may be nulled via connections to the BAL pins. Unlike a voltage feedback amplifier, offset adjustment is accomplished by varying the sign and/or magnitude of the inverting input bias current ( $-I_{BIAS}$ ). With voltage feedback amplifiers, bias currents are matched and bias current induced offset errors are nulled by matching the impedances seen at the positive and negative inputs. Bias

## HS-1120RH

currents are uncorrelated on current feedback amplifiers, so this technique is inappropriate.

$-I_{BIAS}$  flows through  $R_F$  causing an output offset error. Likewise, any change in  $-I_{BIAS}$  forces a corresponding change in output voltage, providing the capability for output offset adjustment. By nulling  $-I_{BIAS}$  to zero, the offset error due to this current is eliminated. In addition, an adjustment limit greater than the  $-I_{BIAS}$  limit allows the user to null the contributions from other error sources, such as  $V_{IO}$ , or  $+IN$

source impedance. For example, the excess adjust current of  $50\mu A [I_{BNADJ} (Min) - I_{BSN} (Max)]$  allows for the nulling of an additional 26mV of output offset error (with  $R_F = 510\Omega$ ) at room temperature. The amount of adjustment is a function of  $R_F$ , so adjust range increases with increased  $R_F$ . If allowed by other considerations, such as bandwidth and noise,  $R_F$  can be increased to provide more adjustment range.

The recommended offset adjustment circuit is shown in Figure 3.

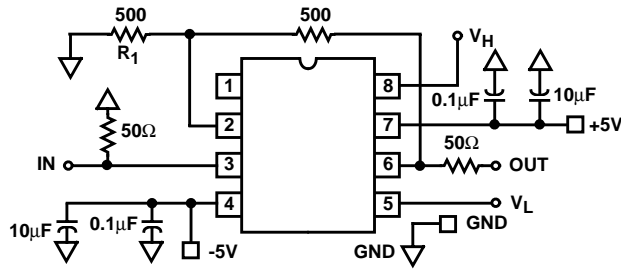


FIGURE 2A. SCHEMATIC

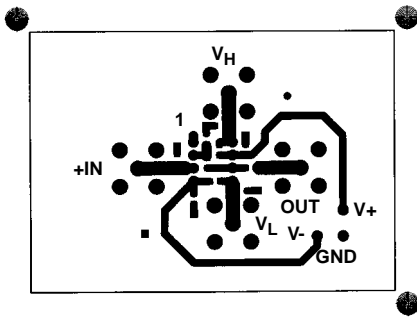


FIGURE 2B. TOP LAYOUT

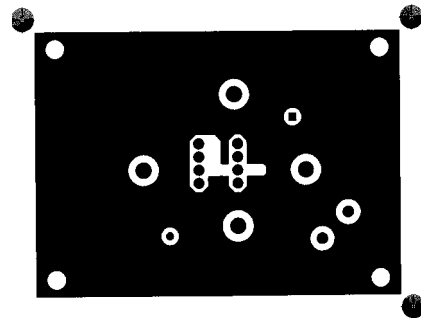


FIGURE 2C. BOTTOM LAYOUT

FIGURE 2. EVALUATION BOARD SCHEMATIC AND LAYOUT

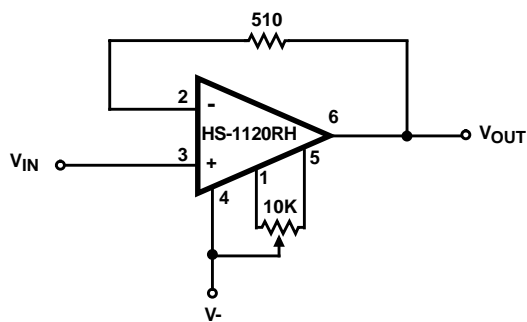


FIGURE 3. OFFSET VOLTAGE ADJUSTMENT CIRCUIT

## HS-1120RH

### Typical Performance Characteristics

Device Characterized at:  $V_{SUPPLY} = \pm 5V$ ,  $R_F = 360\Omega$ ,  $A_V = +2V/V$ ,  $R_L = 100\Omega$ , Unless Otherwise Specified

PARAMETERS	CONDITIONS	TEMPERATURE	TYPICAL	UNITS
Input Offset Voltage (Note 1)	$V_{CM} = 0V$	+25°C	2	mV
Average Offset Voltage Drift	Versus Temperature	Full	10	$\mu V/^\circ C$
$V_{IO}$ CMRR	$\Delta V_{CM} = \pm 2V$	+25°C	46	dB
$V_{IO}$ PSRR	$\Delta V_S = \pm 1.25V$	+25°C	50	dB
+Input Current (Note 1)	$V_{CM} = 0V$	+25°C	25	$\mu A$
Average +Input Current Drift	Versus Temperature	Full	40	$nA/^\circ C$
-Input Current (Note 1)	$V_{CM} = 0V$	+25°C	12	$\mu A$
Average -Input Current Drift	Versus Temperature	Full	40	$nA/^\circ C$
-Input Current Adjust Range	$V_{CM} = 0V$	+25°C	$\pm 200$	$\mu A$
+Input Resistance	$\Delta V_{CM} = \pm 2V$	+25°C	50	k $\Omega$
-Input Resistance		+25°C	16	$\Omega$
Input Capacitance		+25°C	2.2	pF
Input Noise Voltage (Note 1)	f = 100kHz	+25°C	4	$nV/\sqrt{Hz}$
+Input Noise Current (Note 1)	f = 100kHz	+25°C	18	$pA/\sqrt{Hz}$
-Input Noise Current (Note 1)	f = 100kHz	+25°C	21	$pA/\sqrt{Hz}$
Input Common Mode Range		Full	$\pm 3.0$	V
Open Loop Transimpedance	$A_V = -1$	+25°C	500	k $\Omega$
Output Voltage	$A_V = -1$ , $R_L = 100\Omega$	+25°C	$\pm 3.3$	V
	$A_V = -1$ , $R_L = 100\Omega$	Full	$\pm 3.0$	V
Output Current (Note 1)	$A_V = -1$ , $R_L = 50\Omega$	+25°C to +125°C	$\pm 65$	mA
	$A_V = -1$ , $R_L = 50\Omega$	-55°C to 0°C	$\pm 50$	mA
DC Closed Loop Output Resistance		+25°C	0.1	$\Omega$
Quiescent Supply Current (Note 1)	$R_L = \text{Open}$	Full	24	mA
-3dB Bandwidth (Note 1)	$A_V = -1$ , $R_F = 430\Omega$ , $V_{OUT} = 200mV_{P-P}$	+25°C	580	MHz
	$A_V = +1$ , $R_F = 510\Omega$ , $V_{OUT} = 200mV_{P-P}$	+25°C	850	MHz
	$A_V = +2$ , $R_F = 360\Omega$ , $V_{OUT} = 200mV_{P-P}$	+25°C	670	MHz
Slew Rate	$A_V = +1$ , $R_F = 510\Omega$ , $V_{OUT} = 5V_{P-P}$	+25°C	1500	V/ $\mu s$
	$A_V = +2$ , $V_{OUT} = 5V_{P-P}$	+25°C	2300	V/ $\mu s$
Full Power Bandwidth	$V_{OUT} = 5V_{P-P}$	+25°C	220	MHz
Gain Flatness (Note 1)	To 30MHz, $R_F = 510\Omega$	+25°C	$\pm 0.014$	dB
	To 50MHz, $R_F = 510\Omega$	+25°C	$\pm 0.05$	dB
	To 100MHz, $R_F = 510\Omega$	+25°C	$\pm 0.14$	dB
Linear Phase Deviation (Note 1)	To 100MHz, $R_F = 510\Omega$	+25°C	$\pm 0.6$	Degrees
2nd Harmonic Distortion (Note 1)	30MHz, $V_{OUT} = 2V_{P-P}$	+25°C	-55	dBc
	50MHz, $V_{OUT} = 2V_{P-P}$	+25°C	-49	dBc
	100MHz, $V_{OUT} = 2V_{P-P}$	+25°C	-44	dBc
3rd Harmonic Distortion (Note 1)	30MHz, $V_{OUT} = 2V_{P-P}$	+25°C	-84	dBc
	50MHz, $V_{OUT} = 2V_{P-P}$	+25°C	-70	dBc
	100MHz, $V_{OUT} = 2V_{P-P}$	+25°C	-57	dBc
3rd Order Intercept (Note 1)	100MHz, $R_F = 510\Omega$	+25°C	30	dBm
1dB Compression	100MHz, $R_F = 510\Omega$	+25°C	20	dBm
Reverse Isolation ( $S_{12}$ )	40MHz, $R_F = 510\Omega$	+25°C	-70	dB
	100MHz, $R_F = 510\Omega$	+25°C	-60	dB
	600MHz, $R_F = 510\Omega$	+25°C	-32	dB

# HS-1120RH

## Typical Performance Characteristics (Continued)

Device Characterized at:  $V_{SUPPLY} = \pm 5V$ ,  $R_F = 360\Omega$ ,  $A_V = +2V/V$ ,  $R_L = 100\Omega$ , Unless Otherwise Specified (Continued)

PARAMETERS	CONDITIONS	TEMPERATURE	TYPICAL	UNITS
Rise and Fall Time	$V_{OUT} = 0.5V_{P-P}$	+25°C	500	ps
	$V_{OUT} = 2V_{P-P}$	+25°C	800	ps
Overshoot (Note 1)	$V_{OUT} = 0.5V_{P-P}$ , Input $t_R/t_F = 550ps$	+25°C	11	%
Settling Time (Note 1)	To 0.1%, $V_{OUT} = 2V$ to 0V, $R_F = 510\Omega$	+25°C	11	ns
	To 0.05%, $V_{OUT} = 2V$ to 0V, $R_F = 510\Omega$	+25°C	19	ns
	To 0.02%, $V_{OUT} = 2V$ to 0V, $R_F = 510\Omega$	+25°C	34	ns
Differential Gain	$A_V = +2$ , $R_L = 75\Omega$ , NTSC	+25°C	0.03	%
Differential Phase	$A_V = +2$ , $R_L = 75\Omega$ , NTSC	+25°C	0.05	Degrees
Overdrive Recovery Time	$R_F = 510\Omega$ , $V_{IN} = 5V_{P-P}$	+25°C	7.5	ns

NOTE:

- See Typical Performance Curve for more information.

## Typical Performance Curves $V_{SUPPLY} = \pm 5V$ , $R_F = 510\Omega$ , $R_L = 100\Omega$ , $T_A = +25^\circ C$ , Unless Otherwise Specified

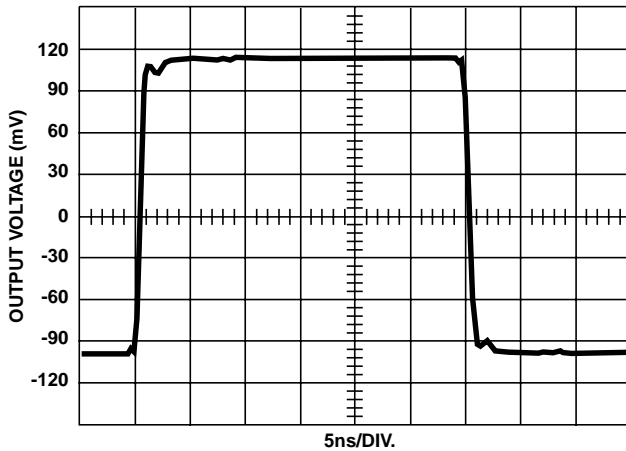


FIGURE 4. SMALL SIGNAL PULSE RESPONSE ( $A_V = +2$ )

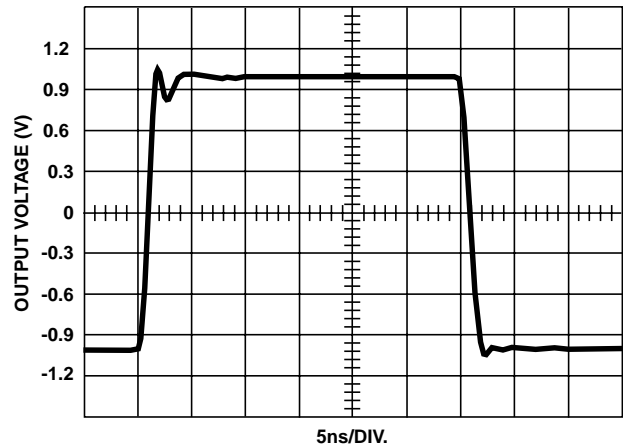


FIGURE 5. LARGE SIGNAL PULSE RESPONSE ( $A_V = +2$ )

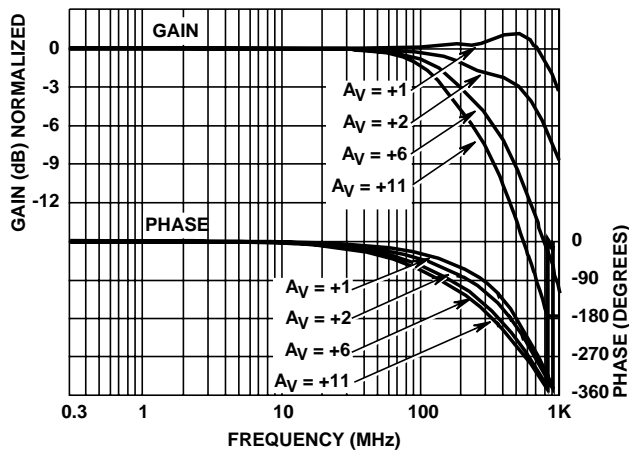


FIGURE 6. NON-INVERTING FREQUENCY RESPONSE ( $V_{OUT} = 200mV_{P-P}$ )

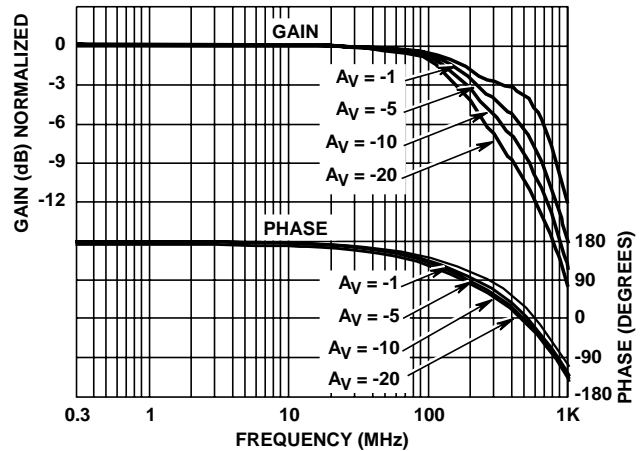


FIGURE 7. INVERTING FREQUENCY RESPONSE ( $V_{OUT} = 200mV_{P-P}$ )

**Typical Performance Curves**  $V_{SUPPLY} = \pm 5V$ ,  $R_F = 510\Omega$ ,  $R_L = 100\Omega$ ,  $T_A = +25^\circ C$ , Unless Otherwise Specified (Continued)

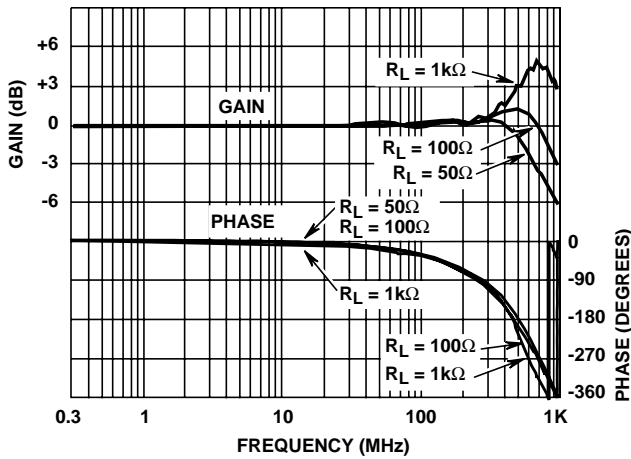


FIGURE 8. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS ( $A_V = +1$ ,  $V_{OUT} = 200mV_{P-P}$ )

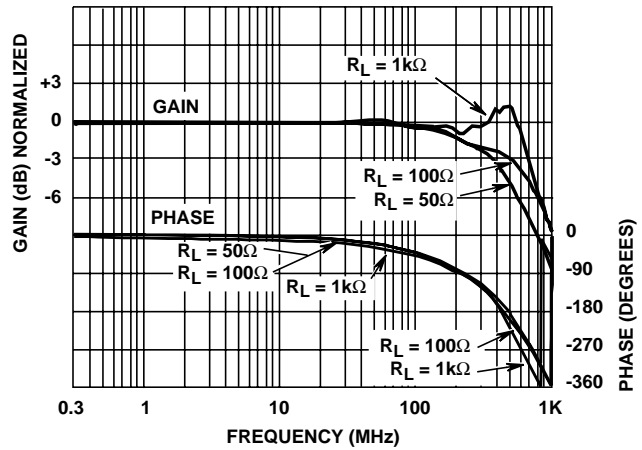


FIGURE 9. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS ( $A_V = +2$ ,  $V_{OUT} = 200mV_{P-P}$ )

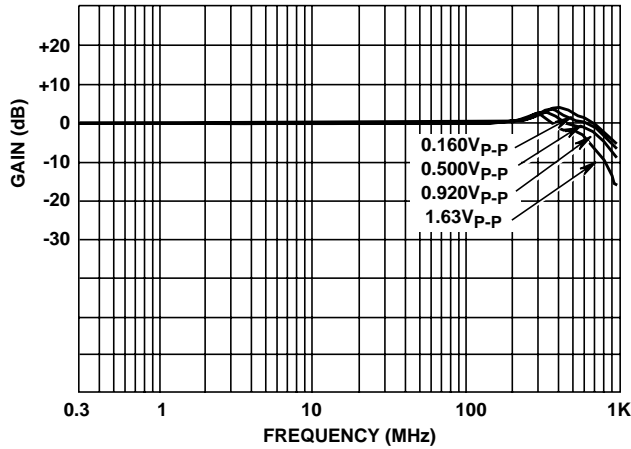


FIGURE 10. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES ( $A_V = +1$ )

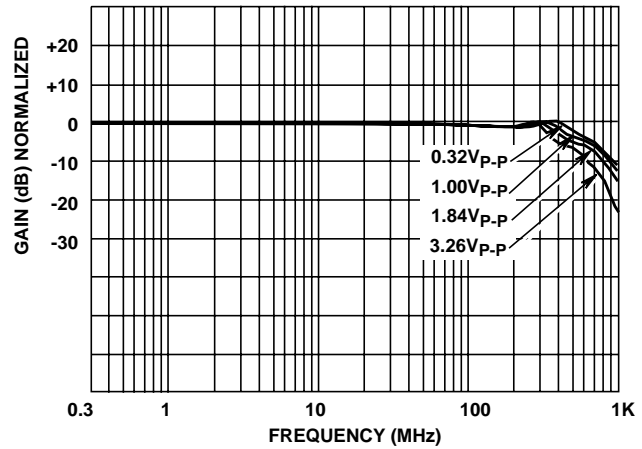


FIGURE 11. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES ( $A_V = +2$ )

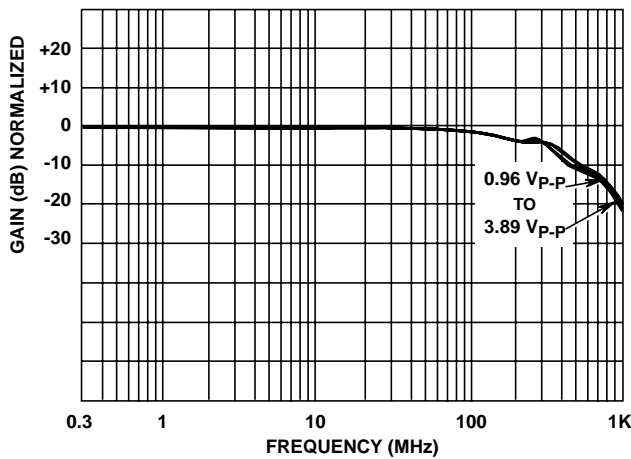


FIGURE 12. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES ( $A_V = +6$ )

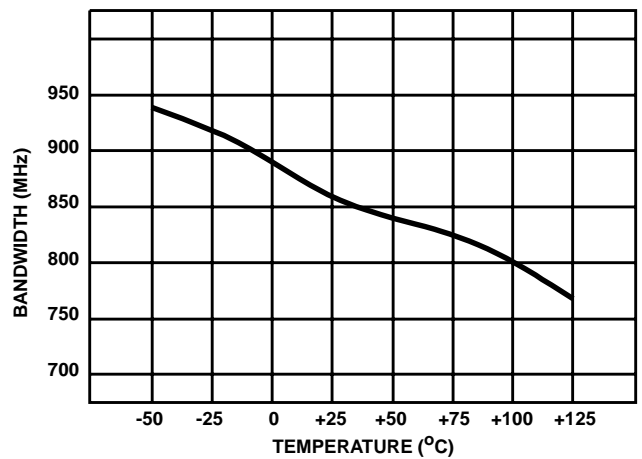


FIGURE 13. -3dB BANDWIDTH vs TEMPERATURE ( $A_V = +1$ )

**Typical Performance Curves**  $V_{SUPPLY} = \pm 5V$ ,  $R_F = 510\Omega$ ,  $R_L = 100\Omega$ ,  $T_A = +25^\circ C$ , Unless Otherwise Specified (Continued)

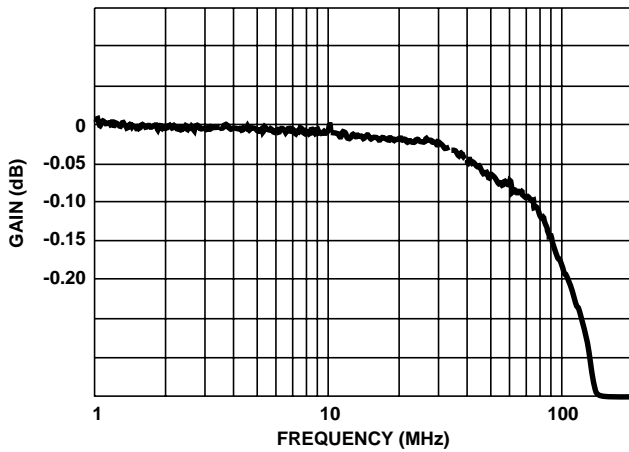


FIGURE 14. GAIN FLATNESS ( $A_V = +2$ )

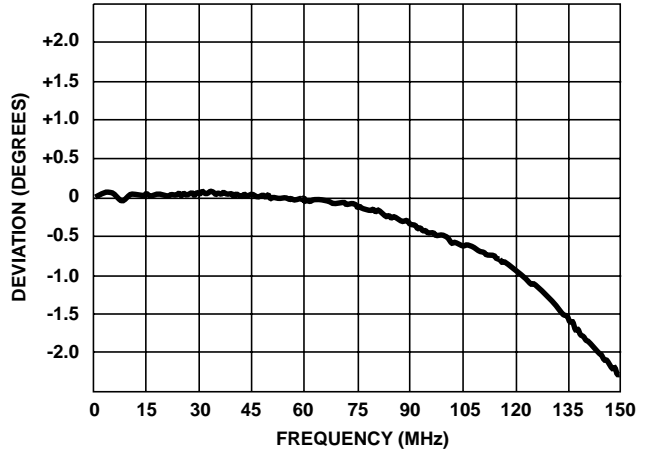


FIGURE 15. DEVIATION FROM LINEAR PHASE ( $A_V = +2$ )

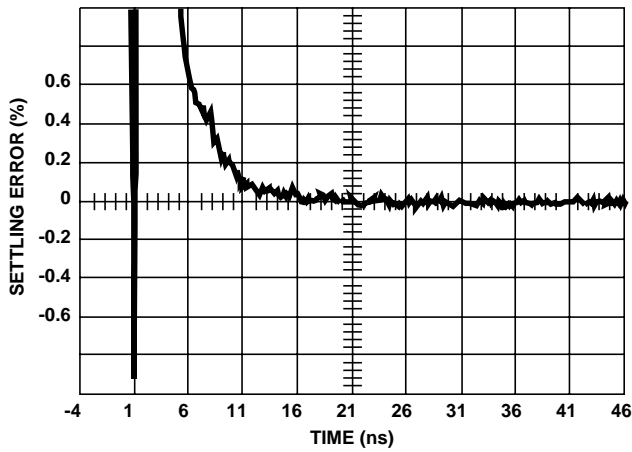


FIGURE 16. SETTLING RESPONSE ( $A_V = +2$ ,  $V_{OUT} = 2V$ )

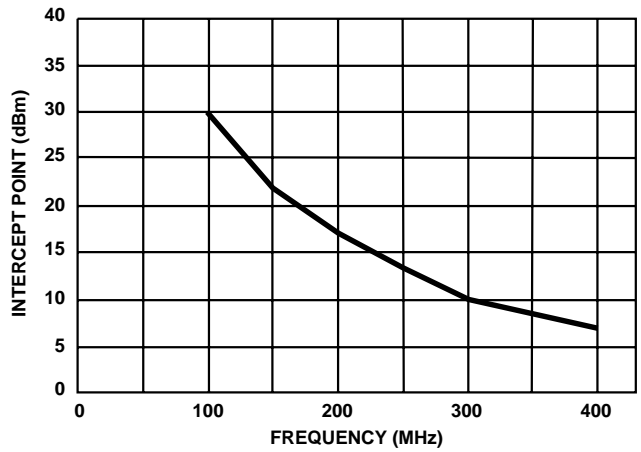


FIGURE 17. 3rd ORDER INTERMODULATION INTERCEPT (2-TONE)

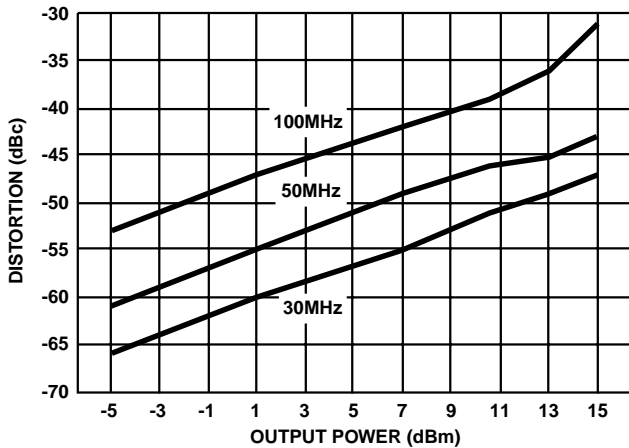


FIGURE 18. 2nd HARMONIC DISTORTION vs  $P_{OUT}$

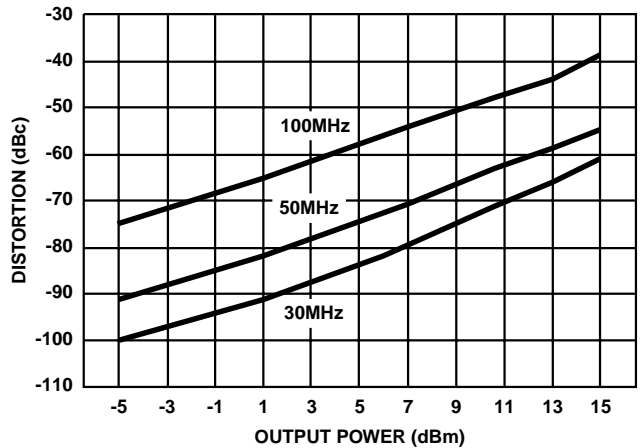


FIGURE 19. 3rd HARMONIC DISTORTION vs  $P_{OUT}$

**Typical Performance Curves**  $V_{SUPPLY} = \pm 5V$ ,  $R_F = 510\Omega$ ,  $R_L = 100\Omega$ ,  $T_A = +25^\circ C$ , Unless Otherwise Specified (Continued)

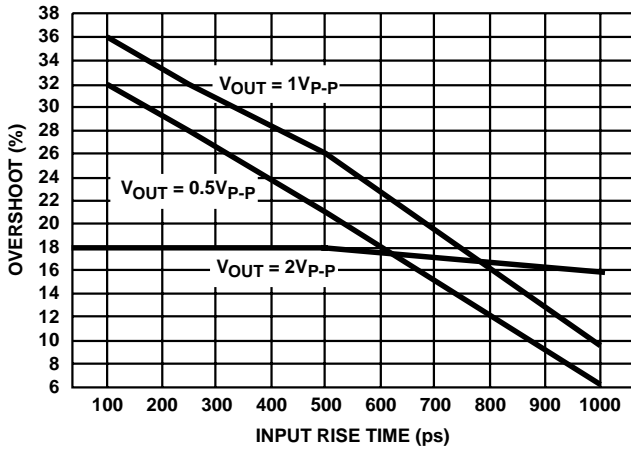


FIGURE 20. OVERSHOOT vs INPUT RISE TIME ( $A_V = +1$ )

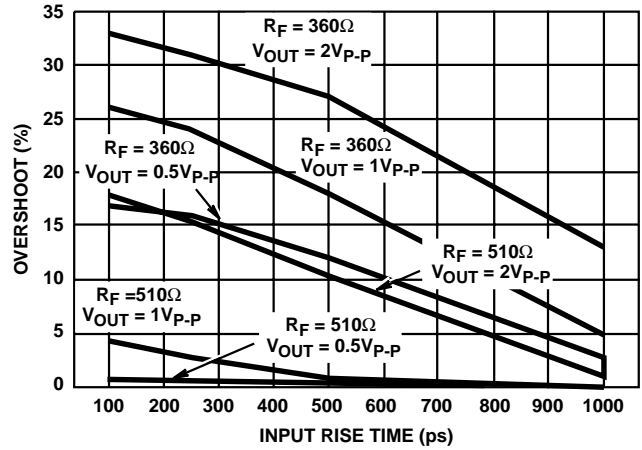


FIGURE 21. OVERSHOOT vs INPUT RISE TIME ( $A_V = +2$ )

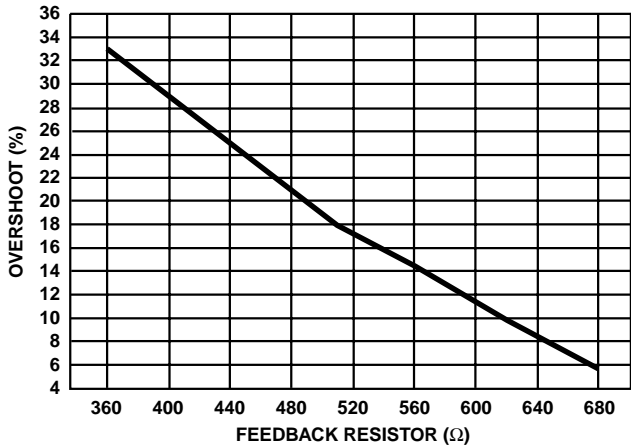


FIGURE 22. OVERSHOOT vs FEEDBACK RESISTOR ( $A_V = +2$ ,  $t_r = 200ps$ ,  $V_{OUT} = 2VP-P$ )

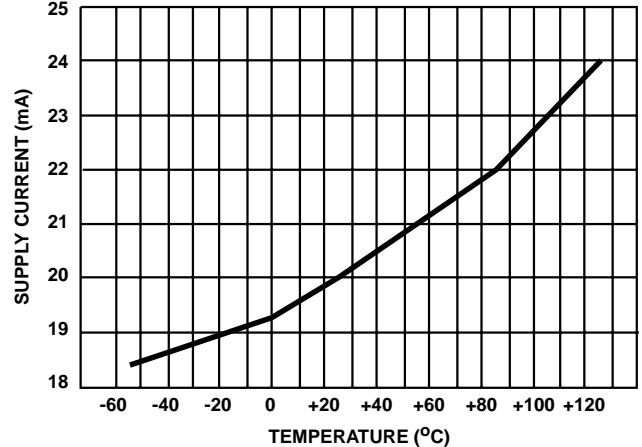


FIGURE 23. SUPPLY CURRENT vs TEMPERATURE

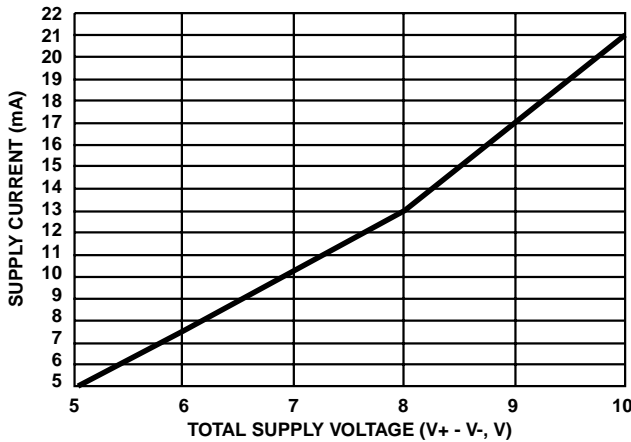


FIGURE 24. SUPPLY CURRENT vs SUPPLY VOLTAGE

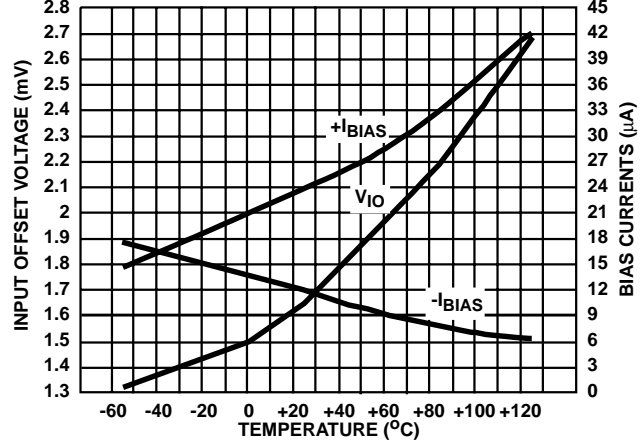


FIGURE 25.  $V_{IO}$  AND BIAS CURRENTS vs TEMPERATURE



# HS-1120RH

**Typical Performance Curves**  $V_{SUPPLY} = \pm 5V$ ,  $R_F = 510\Omega$ ,  $R_L = 100\Omega$ ,  $T_A = +25^\circ C$ , Unless Otherwise Specified (Continued)

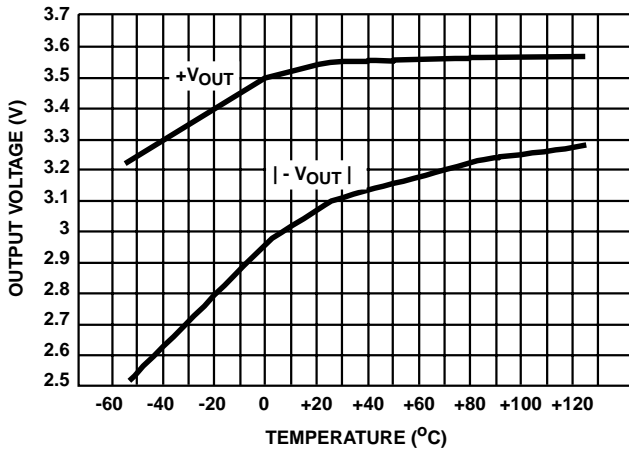


FIGURE 26. OUTPUT VOLTAGE vs TEMPERATURE  
( $A_V = -1$ ,  $R_L = 50\Omega$ )

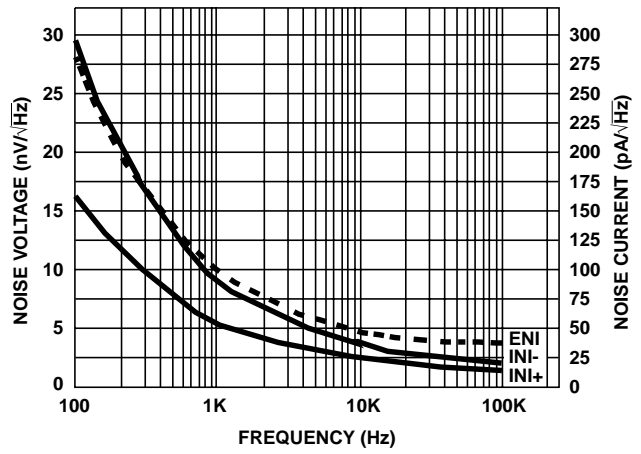
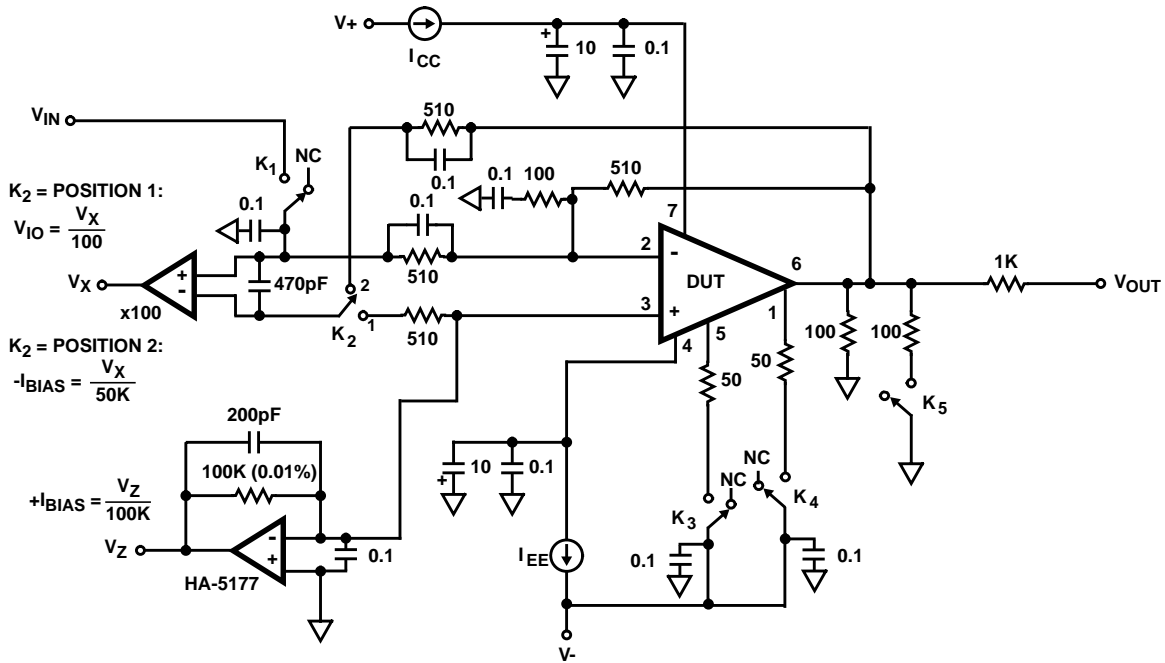


FIGURE 27. INPUT NOISE vs FREQUENCY

## Test Circuit



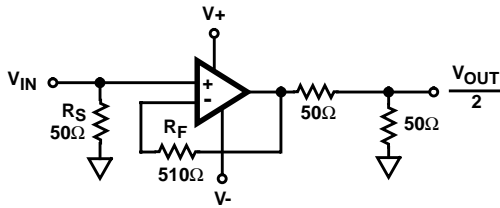
### NOTES:

- All resistors =  $\pm 1\%$  ( $\Omega$ ), unless otherwise noted
- All capacitors =  $\pm 10\%$  ( $\mu F$ ), unless otherwise noted
- Chip Components Recommended

# HS-1120RH

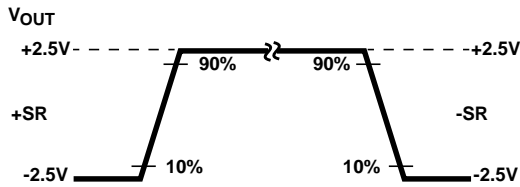
## Test Circuits and Waveforms

### SIMPLIFIED TEST CIRCUIT FOR LARGE AND SMALL SIGNAL PULSE RESPONSE

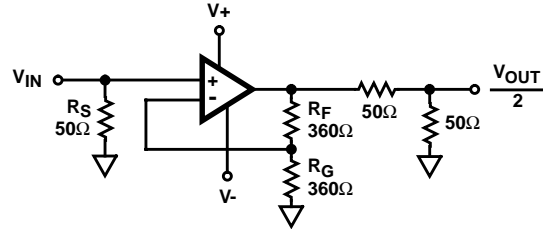


NOTES:  $V_S = \pm 5V$ ,  $A_V = +1$   
 $R_S = 50\Omega$   
 $R_L = 100\Omega$  For Small and Large Signals

**$A_V = +1$  TEST CIRCUIT**

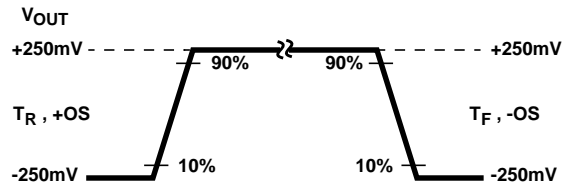


**LARGE SIGNAL WAVEFORM**



NOTES:  $V_S = \pm 5V$ ,  $A_V = +2$   
 $R_S = 50\Omega$   
 $R_L = 100\Omega$  For Small and Large Signals

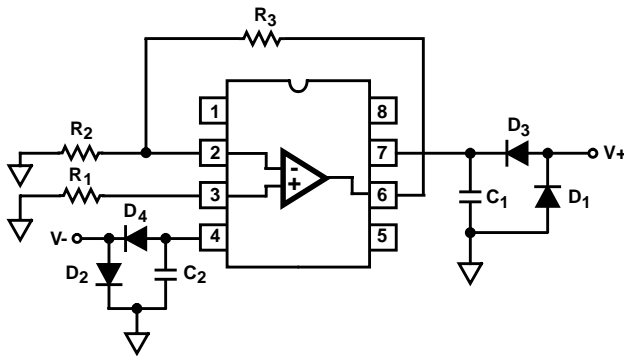
**$A_V = +2$  TEST CIRCUIT**



**SMALL SIGNAL WAVEFORM**

## Burn-In Circuit

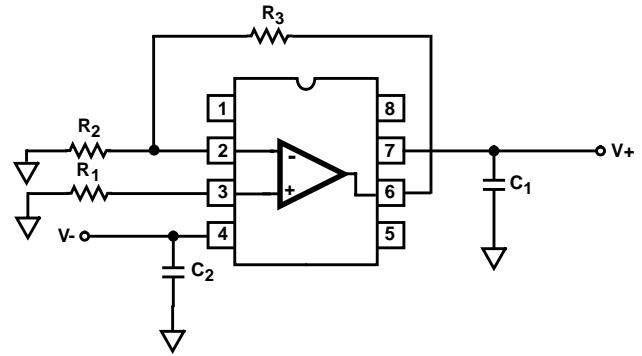
**HS-1120RH CERDIP**



NOTES:  
 $R_1 = R_2 = 1k\Omega, \pm 5\%$  (Per Socket)  
 $R_3 = 10k\Omega, \pm 5\%$  (Per Socket)  
 $C_1 = C_2 = 0.01\mu F$  (Per Socket) or  $0.1\mu F$  (Per Row) Minimum  
 $D_1 = D_2 = 1N4002$  or Equivalent (Per Board)  
 $D_3 = D_4 = 1N4002$  or Equivalent (Per Socket)  
 $V_+ = +5.5V \pm 0.5V$   
 $V_- = -5.5V \pm 0.5V$

## Irradiation Circuit

**HS-1120RH CERDIP**



NOTES:  
 $R_1 = R_2 = 1k\Omega, \pm 5\%$   
 $R_3 = 10k\Omega, \pm 5\%$   
 $C_1 = C_2 = 0.1\mu F$   
 $V_+ = +5.5V \pm 0.5V$   
 $V_- = -5.5V \pm 0.5V$

## HS-1120RH

### Die Characteristics

#### DIE DIMENSIONS:

63 mils x 44 mils x 19 mils  $\pm 1$  mil  
1600 $\mu\text{m}$  x 1130 $\mu\text{m}$  x 483 $\mu\text{m}$   $\pm 25.4\mu\text{m}$

#### METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW  
Thickness: Metal 1: 8k $\text{\AA}$   $\pm 0.4\text{k}\text{\AA}$

Type: Metal 2: AlCu(2%)  
Thickness: Metal 2: 16k $\text{\AA}$   $\pm 0.8\text{k}\text{\AA}$

#### GLASSIVATION:

Type: Nitride  
Thickness: 4k $\text{\AA}$   $\pm 0.5\text{k}\text{\AA}$

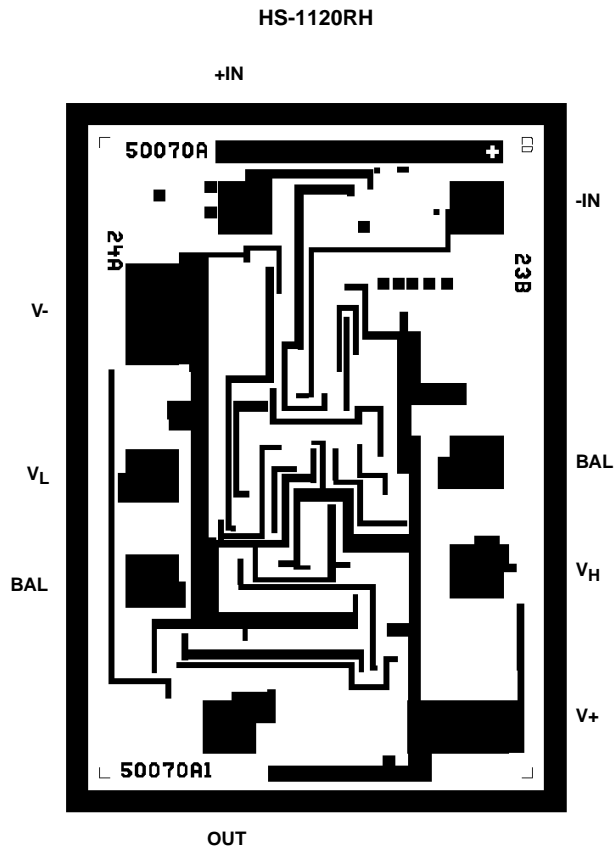
#### WORST CASE CURRENT DENSITY:

1.6 x 10<sup>5</sup> A/cm<sup>2</sup>

#### TRANSISTOR COUNT: 52

**SUBSTRATE POTENTIAL (Powered Up):** Floating

### Metallization Mask Layout



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

*Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>