

**Buck Pulse-Width Modulator (PWM) Controller and Output Voltage Monitor**

The HIP6005B provides complete control and protection for a DC-DC converter optimized for high-performance microprocessor applications. It is designed to drive an N-Channel MOSFET in a standard buck topology. The HIP6005B integrates all of the control, output adjustment, monitoring and protection functions into a single package.

The output voltage of the converter is easily adjusted and precisely regulated. The HIP6005B includes a fully TTL-compatible 5-input digital-to-analog converter (DAC) that adjusts the output voltage from 1.3V<sub>DC</sub> to 2.05V<sub>DC</sub> in 0.05V increments and from 2.1V<sub>DC</sub> to 3.5V<sub>DC</sub> in 0.1V steps. The precision reference and voltage-mode regulator hold the selected output voltage to within ±1% over temperature and line voltage variations.

The HIP6005B provides simple, single feedback loop, voltage-mode control with fast transient response. It includes a 200kHz free-running triangle-wave oscillator that is adjustable from below 50kHz to over 1MHz. The error amplifier features a 15MHz gain-bandwidth product and 6V/μs slew rate which enables high converter bandwidth for fast transient performance. The resulting PWM duty ratio ranges from 0% to 100%.

The HIP6005B monitors the output voltage with a window comparator that tracks the DAC output and issues a Power Good signal when the output is within ±10%. The HIP6005B protects against over-current and over-voltage conditions by inhibiting PWM operation. Additional built-in over-voltage protection triggers an external SCR to crowbar the input supply. The HIP6005B monitors the current by using the r<sub>DS(ON)</sub> of the upper MOSFET which eliminates the need for a current sensing resistor.

**Ordering Information**

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIP6005BCB	0 to 70	20 Ld SOIC	M20.3
HIP6005BCV	0 to 70	20 Ld TSSOP	M20.173

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TSSOP variant in tape and reel, e.g., HIP6005BCV-T.

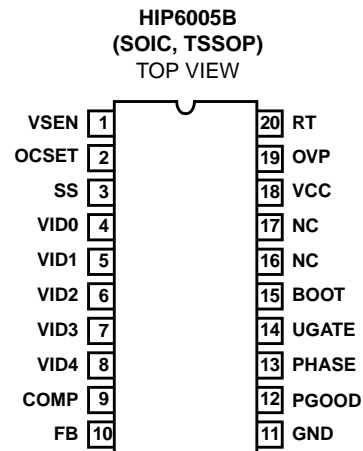
**Features**

- Drives N-Channel MOSFET
- Operates from +5V or +12V Input
- Simple Single-Loop Control Design
  - Voltage-Mode PWM Control
- Fast Transient Response
  - High-Bandwidth Error Amplifier
  - Full 0% to 100% Duty Ratio
- Excellent Output Voltage Regulation
  - ±1% Over Line Voltage and Temperature
- TTL-Compatible 5-Bit Digital-to-Analog Output Voltage Selection
  - Wide Range . . . . . 1.3V<sub>DC</sub> to 3.5V<sub>DC</sub>
  - 0.1V Binary Steps . . . . . 2.1V<sub>DC</sub> to 3.5V<sub>DC</sub>
  - 0.05V Binary Steps . . . . . 1.3V<sub>DC</sub> to 2.05V<sub>DC</sub>
- Power-Good Output Voltage Monitor
- Over-Voltage and Over-Current Fault Monitors
  - Does Not Require Extra Current Sensing Element, Uses MOSFET's r<sub>DS(ON)</sub>
- Small Converter Size
  - Constant Frequency Operation
  - 200kHz Free-Running Oscillator Programmable from 50kHz to over 1MHz

**Applications**

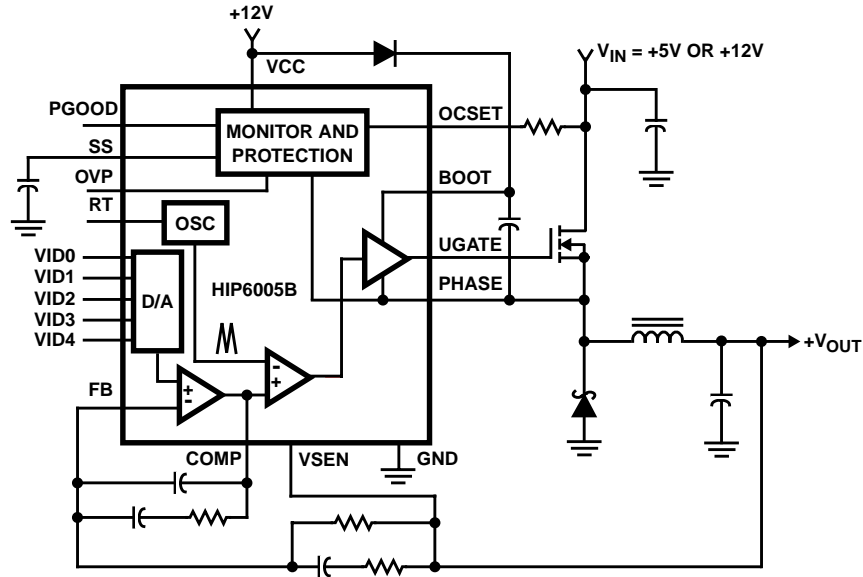
- Power Supply for Pentium®, Pentium Pro, Pentium II, PowerPC™, K6™, 6X86™ and Alpha™ Microprocessors
- High-Power 5V to 3.xV DC-DC Regulators
- Low-Voltage Distributed Power Supplies

**Pinout**

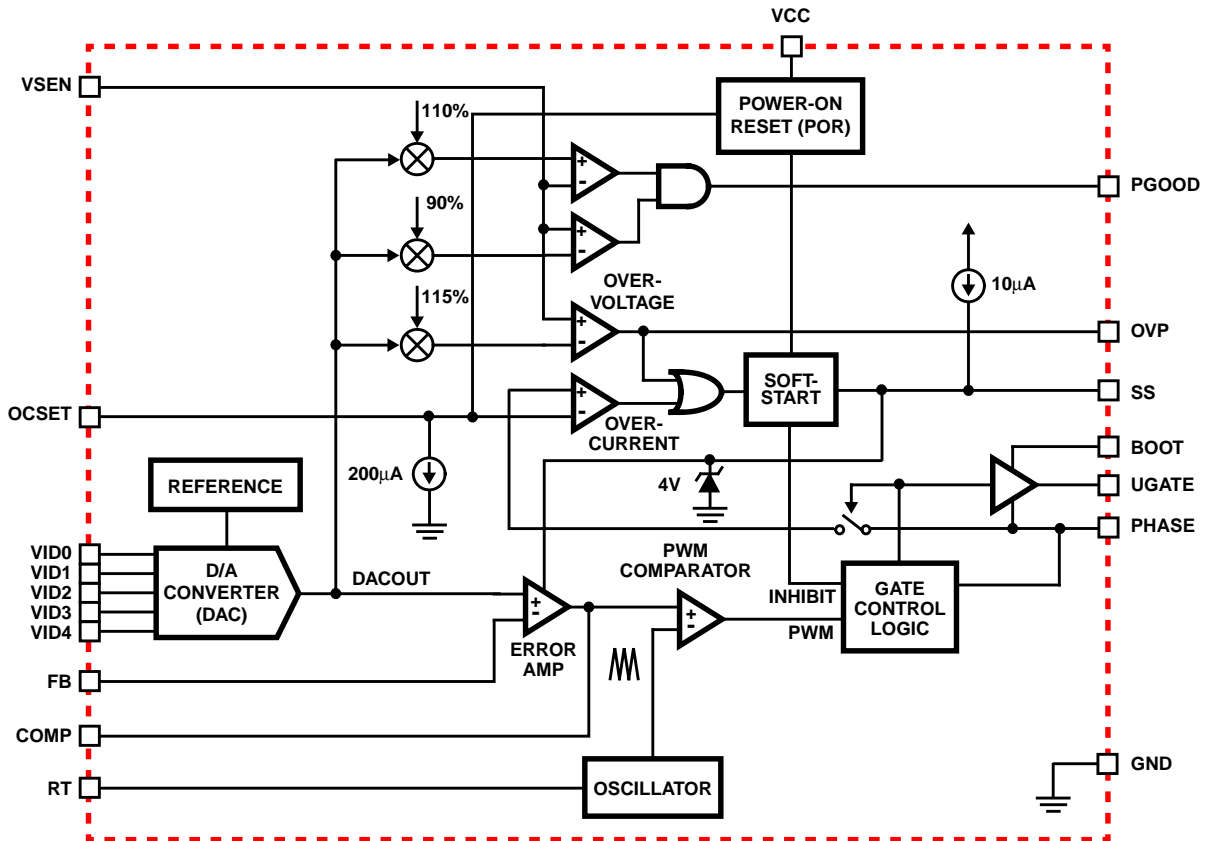


6X86™ is a trademark of Cyrix Corporation.  
 Alpha Micro™ is a trademark of Digital Computer Equipment Corporation  
 K6™ is a trademark of Advanced Micro Devices.  
 Pentium® is a registered trademark of Intel Corporation.  
 PowerPC™ is a registered trademark of IBM.

Typical Application



Block Diagram



# HIP6005B

## Absolute Maximum Ratings

Supply Voltage, $V_{CC}$	+15V
Boot Voltage, $V_{BOOT} - V_{PHASE}$	+15V
Input, Output or I/O Voltage	GND -0.3V to $V_{CC} + 0.3V$
ESD Classification	Class 2

## Operating Conditions

Supply Voltage, $V_{CC}$	+12V $\pm 10\%$
Ambient Temperature Range	0°C to 70°C

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## Thermal Information

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ (°C/W)
SOIC Package	110
SOIC Package (with 3in <sup>2</sup> of Copper)	86
TSSOP Package	140
Maximum Junction Temperature	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C (Lead Tips Only)

## Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b><math>V_{CC}</math> SUPPLY CURRENT</b>						
Nominal Supply	$I_{CC}$	UGATE Open	-	5	-	mA
<b>POWER-ON RESET</b>						
Rising $V_{CC}$ Threshold		$V_{OCSET} = 4.5V$	-	-	10.4	V
Falling $V_{CC}$ Threshold		$V_{OCSET} = 4.5V$	8.2	-	-	V
Rising $V_{OCSET}$ Threshold			-	1.26	-	V
<b>OSCILLATOR</b>						
Free Running Frequency		$R_T = \text{Open}$	185	200	215	kHz
Total Variation		$6k\Omega < R_T \text{ to GND} < 200k\Omega$	-15	-	+15	%
Ramp Amplitude	$\Delta V_{OSC}$	$R_T = \text{Open}$	-	1.9	-	$V_{P-P}$
<b>REFERENCE AND DAC</b>						
DAC (VID0-VID4) Input Low Voltage			-	-	0.8	V
DAC (VID0-VID4) Input High Voltage			2.0	-	-	V
DACOUT Voltage Accuracy			-1.0	-	+1.0	%
<b>ERROR AMPLIFIER</b>						
DC Gain			-	88	-	dB
Gain-Bandwidth Product	GBW		-	15	-	MHz
Slew Rate	SR	COMP = 10pF	-	6	-	$V/\mu s$
<b>GATE DRIVER</b>						
Upper Gate Source	$I_{UGATE}$	$V_{BOOT} - V_{PHASE} = 12V, V_{UGATE} = 6V$	350	500	-	mA
Upper Gate Sink	$R_{UGATE}$		-	5.5	10	W
<b>PROTECTION</b>						
Over-Voltage Trip ( $V_{SEN}/DACOUT$ )			-	115	120	%
OCSET Current Source	$I_{OCSET}$	$V_{OCSET} = 4.5V$	170	200	230	$\mu A$
OVP Sourcing Current	$I_{OVP}$	$V_{SEN} = 5.5V; V_{OVP} = 0V$	60	-	-	mA
Soft Start Current	$I_{SS}$		-	10	-	$\mu A$
<b>POWER GOOD</b>						
Upper Threshold ( $V_{SEN}/DACOUT$ )		$V_{SEN}$ Rising	106	-	111	%
Lower Threshold ( $V_{SEN}/DACOUT$ )		$V_{SEN}$ Falling	89	-	94	%
Hysteresis ( $V_{SEN}/DACOUT$ )		Upper and Lower Threshold	-	2	-	%
PGOOD Voltage Low	$V_{PGOOD}$	$I_{PGOOD} = -5mA$	-	0.5	-	V

Typical Performance Curves

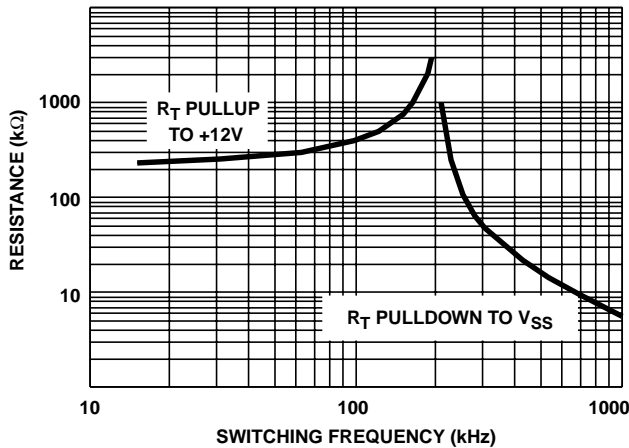


FIGURE 1.  $R_T$  RESISTANCE vs FREQUENCY

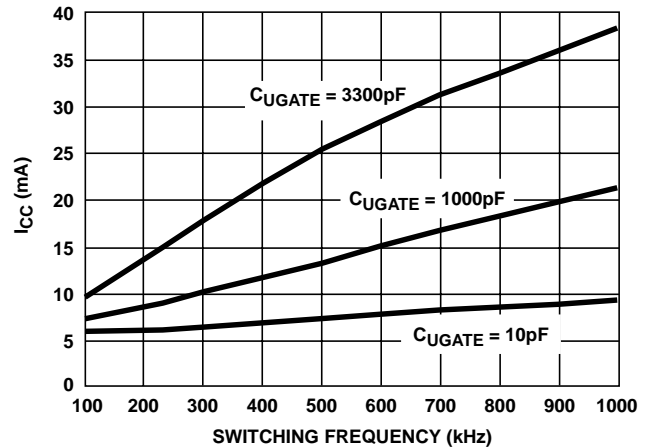
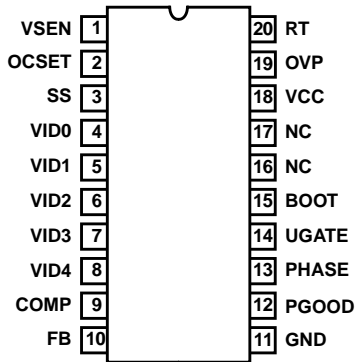


FIGURE 2. BIAS SUPPLY CURRENT vs FREQUENCY

Functional Pin Description



**VSEN (Pin 1)**

This pin is connected to the converters output voltage. The PGOOD and OVP comparator circuits use this signal to report output voltage status and for overvoltage protection.

**OCSET (Pin 2)**

Connect a resistor ( $R_{OCSET}$ ) from this pin to the drain of the upper MOSFET.  $R_{OCSET}$ , an internal  $200\mu A$  current source ( $I_{OCS}$ ), and the upper MOSFET on-resistance ( $r_{DS(ON)}$ ) set the converter over-current (OC) trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}}$$

An over-current trip cycles the soft-start function.

**SS (Pin 3)**

Connect a capacitor from this pin to ground. This capacitor, along with an internal  $10\mu A$  current source, sets the soft-start interval of the converter.

**VID0-4 (Pins 4-8)**

VID0-4 are the input pins to the 5-bit DAC. The states of these five pins program the internal voltage reference (DACOUT). The level of DACOUT sets the converter output voltage. It also sets the PGOOD and OVP thresholds. Table 1 specifies DACOUT for the 32 combinations of DAC inputs.

**COMP (Pin 9) and FB (Pin 10)**

COMP and FB are the available external pins of the error amplifier. The FB pin is the inverting input of the error amplifier and the COMP pin is the error amplifier output. These pins are used to compensate the voltage-control feedback loop of the converter.

**GND (Pin 11)**

Signal ground for the IC. All voltage levels are measured with respect to this pin.

**PGOOD (Pin 12)**

PGOOD is an open collector output used to indicate the status of the converter output voltage. This pin is pulled low when the converter output is not within  $\pm 10\%$  of the DACOUT reference voltage. Exception to this behavior is the '11111' VID pin combination which disables the converter; in this case PGOOD asserts a high level.

**PHASE (Pin 13)**

Connect the PHASE pin to the upper MOSFET source. This pin is used to monitor the voltage drop across the MOSFET for over-current protection. This pin also provides the return path for the upper gate drive.

**UGATE (Pin 14)**

Connect UGATE to the upper MOSFET gate. This pin provides the gate drive for the upper MOSFET.

**BOOT (Pin 15)**

This pin provides bias voltage to the upper MOSFET driver. A bootstrap circuit may be used to create a BOOT voltage suitable to drive a standard N-Channel MOSFET.

**NC (Pin 16)**

No connection.

**NC (Pin 17)**

No connection.

**VCC (Pin 18)**

Provide a 12V bias supply for the chip to this pin.

**OVP (Pin 19)**

The OVP pin can be used to drive an external SCR in the event of an overvoltage condition. Output rising 15% more than the DAC-set voltage triggers a high output on this pin and disables PWM gate drive circuitry.

**RT (Pin 20)**

This pin provides oscillator switching frequency adjustment. By placing a resistor ( $R_T$ ) from this pin to GND, the nominal 200kHz switching frequency is increased according to the following equation:

$$F_s \approx 200\text{kHz} + \frac{5 \times 10^6}{R_T(\text{k}\Omega)} \quad (R_T \text{ to GND})$$

Conversely, connecting a pull-up resistor ( $R_T$ ) from this pin to  $V_{CC}$  reduces the switching frequency according to the following equation:

$$F_s \approx 200\text{kHz} - \frac{4 \times 10^7}{R_T(\text{k}\Omega)} \quad (R_T \text{ to } 12\text{V})$$

**Functional Description**

**Initialization**

The HIP6005B automatically initializes upon receipt of power. Special sequencing of the input supplies is not necessary. The Power-On Reset (POR) function continually monitors the input supply voltages. The POR monitors the bias voltage at the  $V_{CC}$  pin and the input voltage ( $V_{IN}$ ) on the OCSET pin. The level on OCSET is equal to  $V_{IN}$  less a fixed voltage drop (see over-current protection). The POR function initiates soft start operation after both input supply voltages exceed their POR thresholds. For operation with a single +12V power source,  $V_{IN}$  and  $V_{CC}$  are equivalent and the +12V power source must exceed the rising  $V_{CC}$  threshold before POR initiates operation.

**Soft Start**

The POR function initiates the soft start sequence. An internal 10 $\mu$ A current source charges an external capacitor ( $C_{SS}$ ) on the SS pin to 4V. Soft start clamps the error amplifier output (COMP pin) and reference input (+ terminal of error amp) to the SS pin voltage. Figure 3 shows the soft start interval with  $C_{SS} = 0.1\mu\text{F}$ . Initially the clamp on the error amplifier (COMP pin) controls the converter's output voltage. At  $t_1$  in Figure 3,

the SS voltage reaches the valley of the oscillator's triangle wave. The oscillator's triangular waveform is compared to the ramping error amplifier voltage. This generates PHASE pulses of increasing width that charge the output capacitor(s). This interval of increasing pulse width continues to  $t_2$ . With sufficient output voltage, the clamp on the reference input controls the output voltage. This is the interval between  $t_2$  and  $t_3$  in Figure 3. At  $t_3$  the SS voltage exceeds the DACOUT voltage and the output voltage is in regulation. This method provides a rapid and controlled output voltage rise. The PGOOD signal toggles 'high' when the output voltage ( $V_{SEN}$  pin) is within  $\pm 5\%$  of DACOUT. The 2% hysteresis built into the power good comparators prevents PGOOD oscillation due to nominal output voltage ripple.

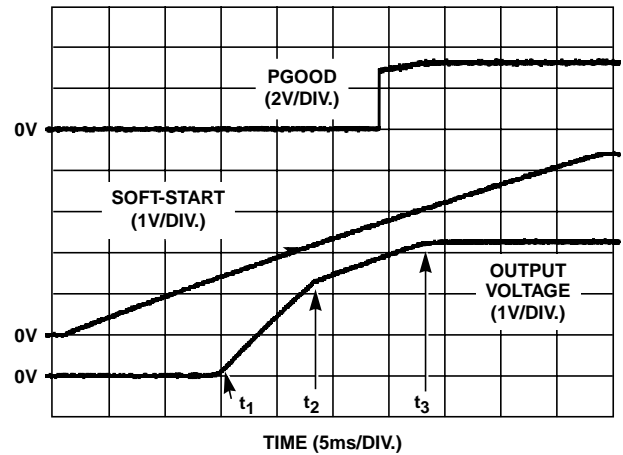


FIGURE 3. SOFT START INTERVAL

**Over-Current Protection**

The over-current function protects the converter from a shorted output by using the upper MOSFET's on-resistance,  $r_{DS(ON)}$  to monitor the current. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor.

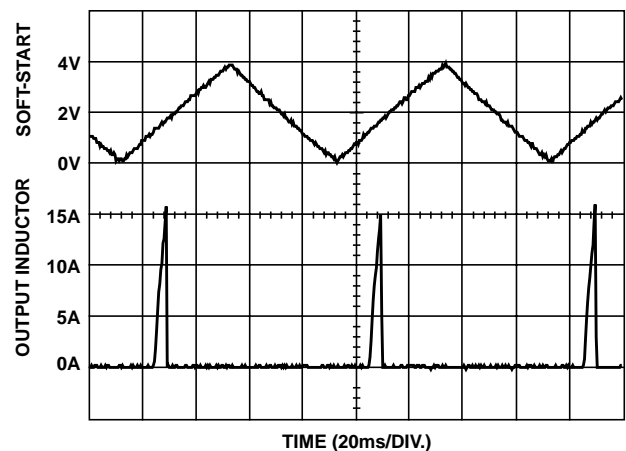


FIGURE 4. OVER-CURRENT OPERATION

The over-current function cycles the soft-start function in a hiccup mode to provide fault protection. A resistor (R<sub>OCSET</sub>) programs the over-current trip level. An internal 200µA current sink develops a voltage across R<sub>OCSET</sub> that is referenced to V<sub>IN</sub>. When the voltage across the upper MOSFET (also referenced to V<sub>IN</sub>) exceeds the voltage across R<sub>OCSET</sub>, the over-current function initiates a soft-start sequence. The soft-start function discharges C<sub>SS</sub> with a 10µA current sink and inhibits PWM operation. The soft-start function recharges C<sub>SS</sub>, and PWM operation resumes with the error amplifier clamped to the SS voltage. Should an overload occur while recharging C<sub>SS</sub>, the soft start function inhibits PWM operation while fully charging C<sub>SS</sub> to 4V to complete its cycle. Figure 4 shows this operation with an overload condition. Note that the inductor current increases to over 15A during the C<sub>SS</sub> charging interval and causes an over-current trip. The converter dissipates very little power with this method. The measured input power for the conditions of Figure 4 is 2.5W.

The over-current function will trip at a peak inductor current (I<sub>PEAK</sub>) determined by:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}}$$

where I<sub>OCSET</sub> is the internal OCSET current source (200µA typical). The OC trip point varies mainly due to the MOSFET's r<sub>DS(ON)</sub> variations. To avoid over-current tripping in the normal operating load range, find the R<sub>OCSET</sub> resistor from the equation above with:

1. The maximum r<sub>DS(ON)</sub> at the highest junction temperature.
2. The minimum I<sub>OCSET</sub> from the specification table.
3. Determine I<sub>PEAK</sub> for I<sub>PEAK</sub> > I<sub>OUT(MAX)</sub> + (ΔI)/2, where ΔI is the output inductor ripple current.

For an equation for the ripple current see the section under component guidelines titled "Output Inductor Selection."

A small ceramic capacitor should be placed in parallel with R<sub>OCSET</sub> to smooth the voltage across R<sub>OCSET</sub> in the presence of switching noise on the input voltage.

### Output Voltage Program

The output voltage of a HIP6005B converter is programmed to discrete levels between 1.8V<sub>DC</sub> and 3.5V<sub>DC</sub>. The voltage identification (VID) pins program an internal voltage reference (DACOUT) with a TTL-compatible, 5-bit digital-to-analog converter (DAC). The level of DACOUT also sets the PGOOD and OVP thresholds. Table 1 specifies the DACOUT voltage for the 32 different combinations of connections on the VID pins. The output voltage should not be adjusted while the converter is delivering power. Remove input power before changing the output voltage. Adjusting the output voltage during operation could toggle the PGOOD signal and exercise the overvoltage protection.

'11111' VID pin combination resulting in a 0V output setting activates the Power-On Reset function and disables the gate drive circuitry. For this specific VID combination, though, PGOOD asserts a high level. This unusual behavior has been implemented in order to allow for operation in dual-microprocessor systems where AND-ing of the PGOOD signals from two individual power converters is implemented.

### Application Guidelines

#### Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible using ground plane construction or single point grounding.

TABLE 1. OUTPUT VOLTAGE PROGRAM

PIN NAME					NOMINAL OUTPUT VOLTAGE DACOUT	PIN NAME					NOMINAL OUTPUT VOLTAGE DACOUT
VID4	VID3	VID2	VID1	VID0		VID4	VID3	VID2	VID1	VID0	
0	1	1	1	1	1.30	1	1	1	1	1	0
0	1	1	1	0	1.35	1	1	1	1	0	2.1
0	1	1	0	1	1.40	1	1	1	0	1	2.2
0	1	1	0	0	1.45	1	1	1	0	0	2.3
0	1	0	1	1	1.50	1	1	0	1	1	2.4
0	1	0	1	0	1.55	1	1	0	1	0	2.5
0	1	0	0	1	1.60	1	1	0	0	1	2.6
0	1	0	0	0	1.65	1	1	0	0	0	2.7
0	0	1	1	1	1.70	1	0	1	1	1	2.8
0	0	1	1	0	1.75	1	0	1	1	0	2.9
0	0	1	0	1	1.80	1	0	1	0	1	3.0
0	0	1	0	0	1.85	1	0	1	0	0	3.1
0	0	0	1	1	1.90	1	0	0	1	1	3.2
0	0	0	1	0	1.95	1	0	0	1	0	3.3
0	0	0	0	1	2.00	1	0	0	0	1	3.4
0	0	0	0	0	2.05	1	0	0	0	0	3.5

NOTE: 0 = connected to GND or V<sub>SS</sub>, 1 = connected to V<sub>DD</sub> through pull-up resistors.

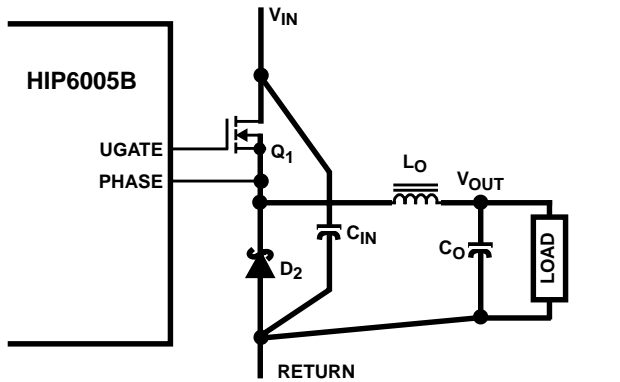


FIGURE 5. PRINTED CIRCUIT BOARD POWER AND GROUND PLANES OR ISLANDS

Figure 5 shows the critical power components of the converter. To minimize the voltage overshoot the interconnecting wires indicated by heavy lines should be part of ground or power plane in a printed circuit board. The components shown in Figure 6 should be located as close together as possible. Please note that the capacitors  $C_{IN}$  and  $C_O$  each represent numerous physical capacitors. Locate the HIP6005B within 3 inches of the MOSFET,  $Q_1$ . The circuit traces for the MOSFET's gate and source connections from the HIP6005B must be sized to handle up to 1A peak current.

Figure 6 shows the circuit traces that require additional layout consideration. Use single point and ground plane construction for the circuits shown. Minimize any leakage current paths on the SS PIN and locate the capacitor,  $C_{SS}$  close to the SS pin because the internal current source is only 10 $\mu$ A. Provide local  $V_{CC}$  decoupling between  $V_{CC}$  and GND pins. Locate the capacitor,  $C_{BOOT}$  as close as practical to the BOOT and PHASE pins.

### Feedback Compensation

Figure 7 highlights the voltage-mode control loop for a buck converter. The output voltage ( $V_{OUT}$ ) is regulated to the Reference voltage level. The error amplifier (Error Amp) output ( $V_{E/A}$ ) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of  $V_{IN}$  at the PHASE node. The PWM wave is smoothed by the output filter ( $L_O$  and  $C_O$ ).

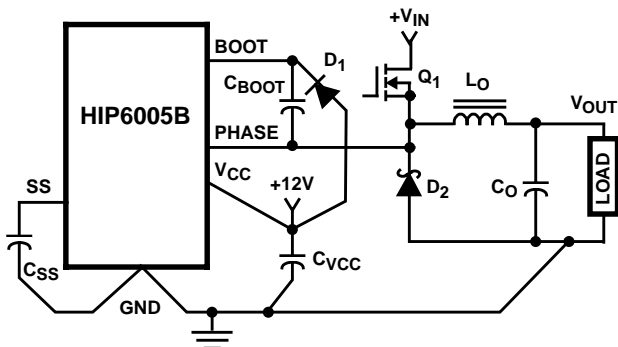


FIGURE 6. PRINTED CIRCUIT BOARD SMALL SIGNAL LAYOUT GUIDELINES

The modulator transfer function is the small-signal transfer function of  $V_{OUT}/V_{E/A}$ . This function is dominated by a DC Gain and the output filter ( $L_O$  and  $C_O$ ), with a double pole break frequency at  $F_{LC}$  and a zero at  $F_{ESR}$ . The DC Gain of the modulator is simply the input voltage ( $V_{IN}$ ) divided by the peak-to-peak oscillator voltage  $\Delta V_{OSC}$ .

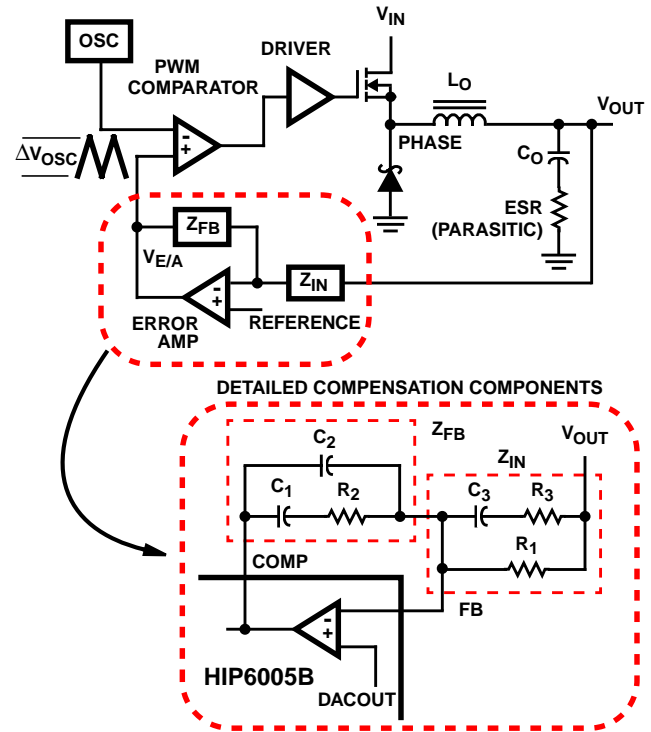


FIGURE 7. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

### Modulator Break Frequency Equations

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \quad F_{ESR} = \frac{1}{2\pi \times (ESR \times C_O)}$$

The compensation network consists of the error amplifier (internal to the HIP6005B) and the impedance networks  $Z_{IN}$  and  $Z_{FB}$ . The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency ( $f_{0dB}$ ) and adequate phase margin. Phase margin is the difference between the closed loop phase at  $f_{0dB}$  and 180 degrees. The equations below relate the compensation network's poles, zeros and gain to the components ( $R_1$ ,  $R_2$ ,  $R_3$ ,  $C_1$ ,  $C_2$ , and  $C_3$ ) in Figure 8. Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick Gain ( $R_2/R_1$ ) for desired converter bandwidth.
2. Place 1<sup>ST</sup> Zero Below Filter's Double Pole ( $\sim 75\% F_{LC}$ ).
3. Place 2<sup>ND</sup> Zero at Filter's Double Pole.
4. Place 1<sup>ST</sup> Pole at the ESR Zero.
5. Place 2<sup>ND</sup> Pole at Half the Switching Frequency.
6. Check Gain against Error Amplifier's Open-Loop Gain.
7. Estimate Phase Margin - Repeat if Necessary.

**Compensation Break Frequency Equations**

$$F_{Z1} = \frac{1}{2\pi \times R_2 \times C_1} \quad F_{P1} = \frac{1}{2\pi \times R_2 \times \left(\frac{C_1 \times C_2}{C_1 + C_2}\right)}$$

$$F_{Z2} = \frac{1}{2\pi \times (R_1 + R_3) \times C_3} \quad F_{P2} = \frac{1}{2\pi \times R_3 \times C_3}$$

Figure 8 shows an asymptotic plot of the DC-DC converter's gain vs frequency. The actual Modulator Gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 8. Using the above guidelines should give a Compensation Gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at  $F_{P2}$  with the capabilities of the error amplifier. The Closed Loop Gain is constructed on the log-log graph of Figure 8 by adding the Modulator Gain (in dB) to the Compensation Gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

The compensation gain uses external impedance networks  $Z_{FB}$  and  $Z_{IN}$  to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45 degrees. Include worst case component variations when determining phase margin.

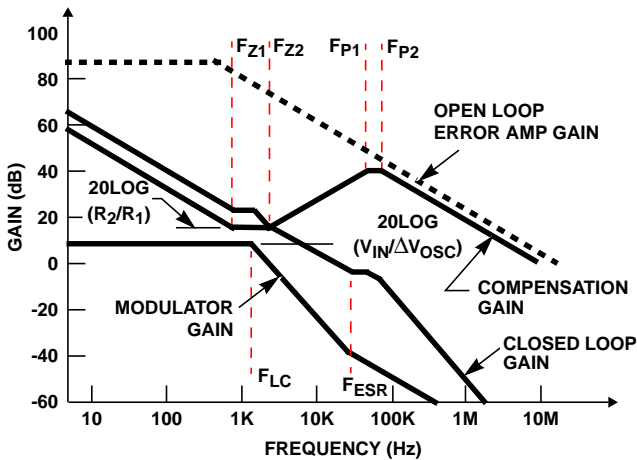


FIGURE 8. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

**Component Selection Guidelines**

**Output Capacitor Selection**

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Modern microprocessors produce transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements. For example, Intel recommends that the high frequency decoupling for the Pentium Pro be composed of at least forty (40) 1μF ceramic capacitors in the 1206 surface-mount package.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the Equivalent Series Inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

**Output Inductor Selection**

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{F_S \times L} \times \frac{V_{OUT}}{V_{IN}} \quad \Delta V_{OUT} = \Delta I \times ESR$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.



One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the HIP6005B will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L \times I_{TRAN}}{V_{IN} - V_{OUT}} \quad t_{FALL} = \frac{L \times I_{TRAN}}{V_{OUT}}$$

where:  $I_{TRAN}$  is the transient load current step,  $t_{RISE}$  is the response time to the application of load, and  $t_{FALL}$  is the response time to the removal of load. With a +5V input source, the worst case response time can be either at the application or removal of load and dependent upon the DACOUT setting. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time. With a +12V input, and output voltage level equal to DACOUT,  $t_{FALL}$  is the longest response time.

### Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time  $Q_1$  turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of  $Q_1$  and the anode of Schottky diode  $D_2$ .

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

For a through hole design, several electrolytic capacitors (Panasonic HFQ series or Nichicon PL series or Sanyo MV-GX or equivalent) may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

### MOSFET Selection/Considerations

The HIP6005B requires an N-Channel power MOSFET. It should be selected based upon  $r_{DS(ON)}$ , gate supply requirements, and thermal management requirements.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for the MOSFET. Switching losses also contribute to the overall MOSFET power loss (see the equations below). These equations assume linear voltage-current transitions and are approximations. The gate-charge losses are dissipated by the HIP6005B and do not heat the MOSFET. However, large gate-charge increases the switching interval,  $t_{SW}$ , which increases the upper MOSFET switching losses. Ensure that the MOSFET is within its maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

$$P_{COND} = I_O^2 \times r_{DS(ON)} \times D$$

$$P_{SW} = 1/2 I_O \times V_{IN} \times t_{SW} \times F_S$$

Where:  $D$  is the duty cycle =  $V_{OUT}/V_{IN}$ ,

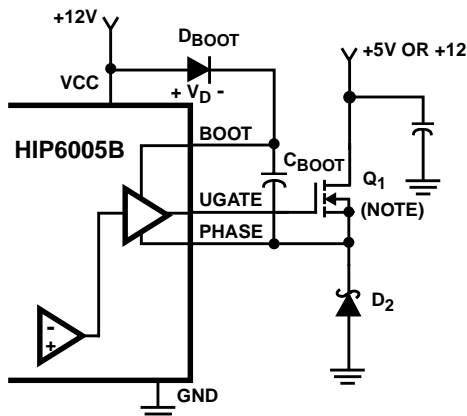
$t_{SW}$  is the switching interval, and

$F_S$  is the switching frequency

Standard-gate MOSFETs are normally recommended for use with the HIP6005B. However, logic-level gate MOSFETs can be used under special circumstances. The input voltage, upper gate drive level, and the MOSFETs absolute gate-to-source voltage rating determine whether logic-level MOSFETs are appropriate.

Figure 9 shows the upper gate drive (BOOT pin) supplied by a bootstrap circuit from  $V_{CC}$ . The boot capacitor,  $C_{BOOT}$ , develops a floating supply voltage referenced to the PHASE pin. This supply is refreshed each cycle to a voltage of  $V_{CC}$  less the boot diode drop ( $V_D$ ) when the Schottky diode,  $D_2$ , conducts. Logic-level MOSFETs can only be used if the MOSFETs absolute gate-to-source voltage rating exceeds the maximum voltage applied to  $V_{CC}$ .

Figure 10 shows the upper gate drive supplied by a direct connection to  $V_{CC}$ . This option should only be used in converter systems where the main input voltage is +5V<sub>DC</sub> or less. The peak upper gate-to-source voltage is approximately  $V_{CC}$  less the input supply. For +5V main power and +12V<sub>DC</sub> for the bias, the gate-to-source voltage of  $Q_1$  is 7V. A logic-level MOSFET is a good choice for  $Q_1$  under these conditions.



NOTE:  $V_{G-S} \approx V_{CC} - V_D$ .

FIGURE 9. UPPER GATE DRIVE - BOOTSTRAP OPTION

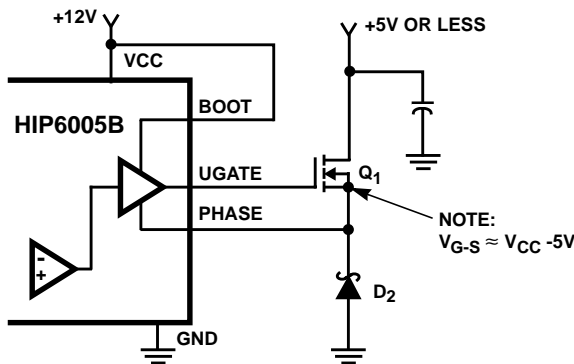


FIGURE 10. UPPER GATE DRIVE - DIRECT  $V_{CC}$  DRIVE OPTION

### Schottky Selection

Rectifier  $D_2$  conducts when the upper MOSFET  $Q_1$  is off. The diode should be a Schottky type for low power losses. The power dissipation in the Schottky rectifier is approximated by:

$$P_{COND} = I_0 \times V_f \times (1 - D)$$

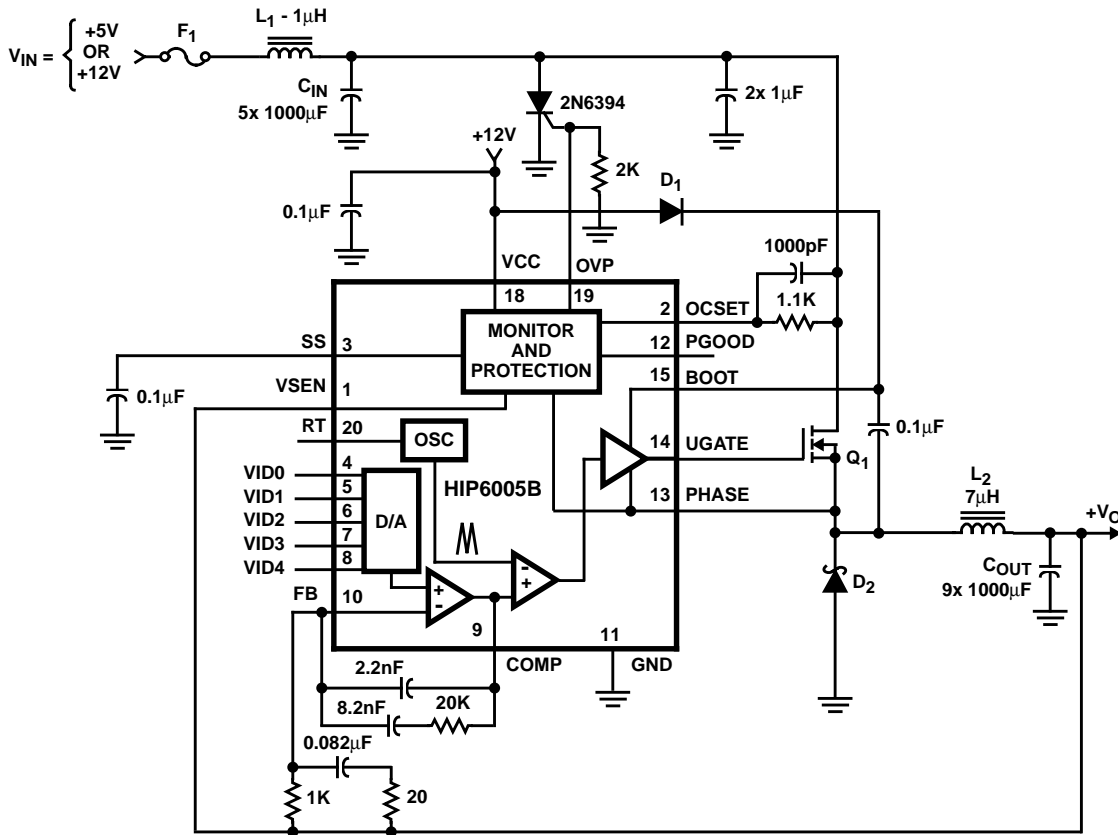
Where:  $D$  is the duty cycle =  $V_{OUT} / V_{IN}$ , and  $V_f$  is the Schottky forward voltage drop.

In addition to power dissipation, package selection and heat-sink requirements are the main design tradeoffs in choosing the schottky rectifier. Since the three factors are interrelated, the selection process is an iterative procedure. The maximum junction temperature of the rectifier must remain below the manufacturer's specified value, typically  $125^{\circ}\text{C}$ . By using the package thermal resistance specification and the schottky power dissipation equation (shown above), the junction temperature of the rectifier can be estimated. Be sure to use the available airflow and ambient temperature to determine the junction temperature rise.

**HIP6005B DC-DC Converter Application Circuit**

Figure 11 shows an application circuit of a DC-DC Converter for an Intel Pentium Pro microprocessor. Detailed information on the circuit, including a complete Bill-of-Materials and circuit board description, can be found in

application note AN9706. Although the Application Note details the HIP6005, the same evaluation platform can be used to evaluate the HIP6005B. Intersil AnswerFAX (407-724-7800) Doc. #99706.



**Component Selection Notes**

C<sub>OUT</sub> - Each 1000µF 6.3WV<sub>DC</sub>, Sanyo MV-GX or Equivalent.

C<sub>IN</sub> - Each 330µF 25WV<sub>DC</sub>, Sanyo MV-GX or Equivalent.

L<sub>2</sub> - Core: Micrometals T60-52; Each Winding: 14 Turns of 17AWG.

L<sub>1</sub> - Core: Micrometals T50-52; Winding: 6 Turns of 18AWG.

D<sub>1</sub> - 1N4148 or Equivalent.

D<sub>2</sub> - 25A, 35V Schottky, Motorola MBR2535CTL or Equivalent.

Q<sub>1</sub> - Intersil MOSFET; RFP70N03.

**FIGURE 11. PENTIUM PRO DC-DC CONVERTER**

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