

**8-Bit, 120MSPS, Flash A/D Converter**

The HI3256 is an 8-bit, high-speed, flash analog-to-digital converter optimized for high speed, low power, and ease of use. With a 120MSPS encode rate capability and full-power analog bandwidth of 250MHz, this component is ideal for applications requiring the highest possible dynamic performance.

To minimize system cost and power dissipation, only a +5V power supply is required. The HI3256 clock input interfaces directly to TTL, ECL or PECL logic and will operate with single-ended inputs. The user may select 16-bit demultiplexed output or 8-bit single channel digital outputs. The demultiplexed mode interleaves the data through two 8-bit channels at <sup>1</sup>/<sub>2</sub> the clock rate. Operation in demultiplexed mode reduces the speed and cost of external digital interfaces, while allowing the A/D converter to be clocked to the full 120MSPS conversion rate.

Fabricated with an advanced Bipolar process, the HI3256 is provided in a space-saving 48-lead LQFP surface mount plastic package and is specified over the -20°C to 75°C temperature range.

**Ordering Information**

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI3256JCQ	-20 to 75	48 Ld LQFP	Q48.7x7-S

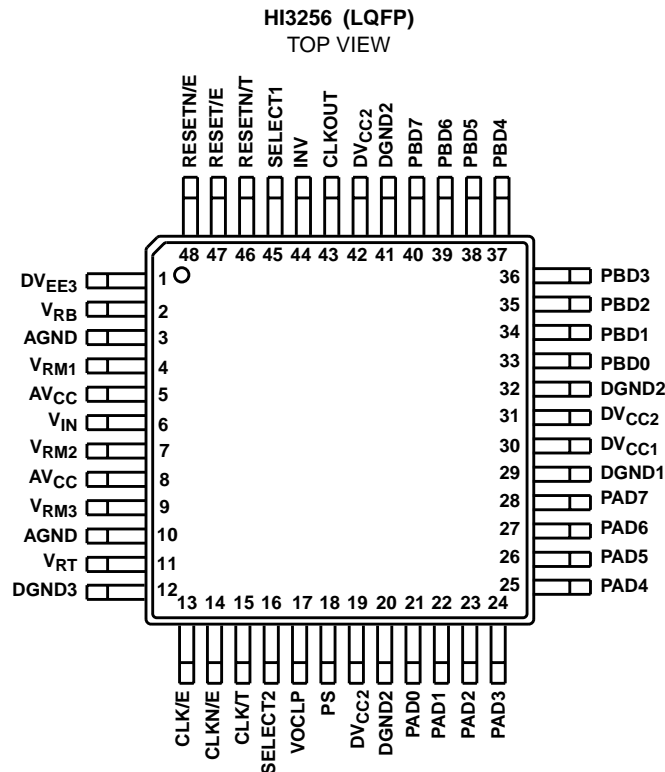
**Features**

- Differential Linearity Error . . . . . ±0.5 LSB
- Integral Linearity Error . . . . . ±0.5 LSB
- Low Input Capacitance . . . . . 10pF
- Wide Analog Input Bandwidth . . . . . 250MHz
- Low Power Consumption . . . . . 500mW
- Output Voltage Control Function (VOCLP pin)
- 1:2 Demultiplexed Output Pin
- Internal <sup>1</sup>/<sub>2</sub> Frequency Divider Circuit (w/Reset Function)
- CLK/2 Clock Output
- Compatible with PECL, ECL and TTL Digital Input Levels
- Direct Replacement for Sony CXA3256R

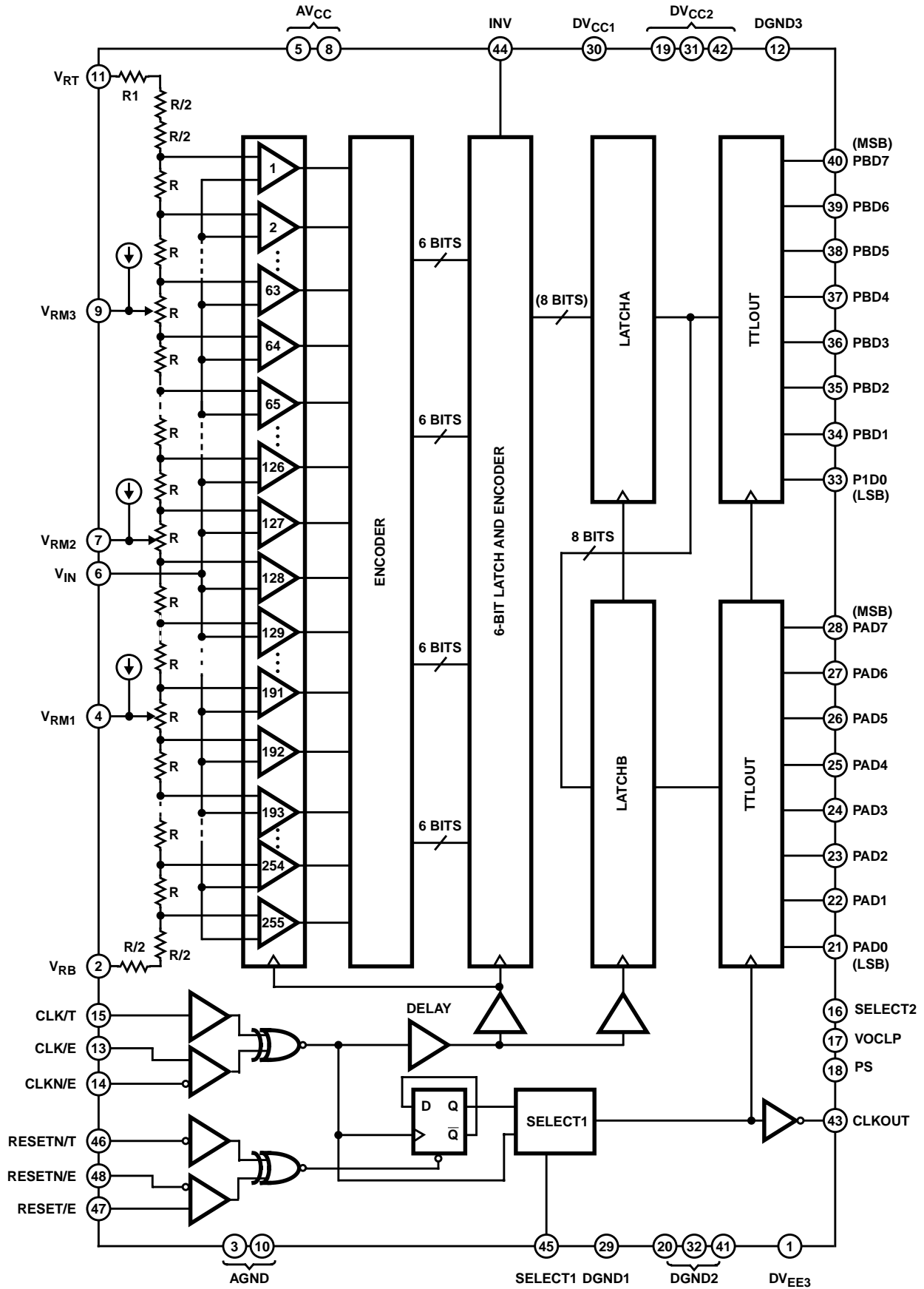
**Applications**

- LCD/PDP Monitors and Projectors (RGB Video)
- Digital Oscilloscopes
- Digital Communications (QPSK, QAM)
- Magnetic Recording (PRML)

**Pinout**



Block Diagram



**Absolute Maximum Ratings**  $T_A = 25^{\circ}\text{C}$

Supply Voltage ( $AV_{CC}$ , $DV_{CC1}$ , $DV_{CC2}$ )	.....	-0.5V to +7.0V
(DGND3)	.....	-0.5V to +7.0V
( $DV_{EE3}$ )	.....	-7.0V to +0.5V
(DGND3 - $DV_{EE3}$ )	.....	-0.5V to +7.0V
Analog Input Voltage ( $V_{IN}$ )	.....	$V_{RT} - 2.7V$ to $AV_{CC}$
Reference Input Voltage ( $V_{RT}$ )	.....	+2.7V to $AV_{CC}$
( $V_{RB}$ )	.....	$V_{IN} - 2.7V$ to $AV_{CC}$
( $ V_{RT} - V_{RB} $ )	.....	+2.5V
Digital Input Voltage		
PECL/ECL	.....	$DV_{EE3} - 0.5$ to DGND3 + 0.5
TTL	.....	DGND3 - 0.5 to $DV_{CC1}$ + 0.5
$V_{ID}$ ( $ ^{**}/E - ^{***}N/E $ (Note 2))	.....	2.7V

**Thermal Information**

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ ( $^{\circ}\text{C}/\text{W}$ )
LQFP Package	65
Maximum Junction Temperature	150 $^{\circ}\text{C}$
Maximum Storage Temperature Range	-65 $^{\circ}\text{C}$ to 150 $^{\circ}\text{C}$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}\text{C}$
(Lead Tips Only)	

**Recommended Operating Conditions**

WITH A SINGLE POWER SUPPLY	MIN	TYP	MAX	WITH DUAL POWER SUPPLIES	MIN	TYP	MAX
Supply Voltage				Supply Voltage			
$DV_{CC1}$ , $DV_{CC2}$ , $AV_{CC}$	+4.75	+5.0	+5.25V	$DV_{CC1}$ , $DV_{CC2}$ , $AV_{CC}$	+4.75	+5.0	+5.25V
DGND1, DGND2, AGND	-0.05	0	+0.05V	DGND1, DGND2, AGND	-0.05	0	+0.05V
DGND3	+4.75	+5.0	+5.25V	DGND3	-0.05	0	+0.05V
$DV_{EE3}$	-0.05	0	+0.05V	$DV_{EE3}$	-5.5	-5.0	-4.75V
Analog Input Voltage ( $V_{IN}$ )	$V_{RB}$	-	$V_{RT}$	Analog Input Voltage ( $V_{IN}$ )	$V_{RB}$	-	$V_{RT}$
Reference Input Voltage				Reference Input Voltage			
$V_{RT}$	+2.9	-	+4.1V	$V_{RT}$	+2.9	-	+4.1V
$V_{RB}$	+1.4	-	+2.6V	$V_{RB}$	+1.4	-	+2.6V
$ V_{RT} - V_{RB} $	+1.5	-	+2.1V	$ V_{RT} - V_{RB} $	+1.5	-	+2.1V
Digital Input Voltage				Digital Input Voltage			
PECL ( $^{**}/E$ ) $V_{IH}$	$DV_{EE3} + 1.5$	DGND3		PECL/ECL $V_{IH}$	$DV_{EE3} + 1.5$	DGND3	
PECL ( $^{**}/E$ ) $V_{IL}$	$DV_{EE3} + 1.1$	$V_{IH} - 0.4V$		PECL/ECL $V_{IL}$	$DV_{EE3} + 1.1$	$V_{IH} - 0.4$	
TTL ( $^{**}/T$ , INV) $V_{IH}$	+2.0V	-	-	TTL ( $^{**}/T$ , INV) $V_{IH}$	2.0	-	-
TTL ( $^{**}/T$ , INV) $V_{IL}$	-	-	+0.8V	TTL ( $^{**}/T$ , INV) $V_{IL}$	-	-	+0.8V
Other (SELECT1/2) $V_{IH}$	-	$DV_{CC1}$	-	Other (SELECT1/2) $V_{IH}$	-	$DV_{CC1}$	-
Other (SELECT1/2) $V_{IL}$	-	DGND1	-	Other (SELECT1/2) $V_{IL}$	-	DGND1	-
$V_{ID}$ (Note 2) ( $ ^{**}/E - ^{***}N/E $ )	+0.4	+0.8	-	$V_{ID}$ (Note 2) ( $ ^{**}/E - ^{***}N/E $ )	+0.4	0.8	-
Max Conversion Rate ( $f_C$ , Straight Mode)	100	-	-	Max Conversion Rate ( $f_C$ , Straight Mode)	100	-	-
	MSPS				MSPS		
Max Conversion Rate ( $f_C$ , DMUX Mode)	120	-	-	Max Conversion Rate ( $f_C$ , DMUX Mode)	120	-	-
	MSPS				MSPS		
Ambient Temperature ( $T_A$ )	-20 $^{\circ}\text{C}$ to 75 $^{\circ}\text{C}$			Ambient Temperature ( $T_A$ )	-20 $^{\circ}\text{C}$ to 75 $^{\circ}\text{C}$		

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.
- $V_{ID}$ : Input Voltage Differential.

**Electrical Specifications**  $DV_{CC1, 2}$ ,  $AV_{CC}$ , DGND3 = +5V, DGND1, 2, AGND,  $DV_{EE3} = 0V$ ,  $V_{RT} = 4V$ ,  $V_{RB} = 2V$ ,  $T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		-	8	-	Bits
<b>DC CHARACTERISTICS</b>					
Integral Linearity Error, INL	$V_{IN} = 2V_{P-P}$ , $f_C = 5\text{MSPS}$	-	-	$\pm 0.5$	LSB
Differential Linearity Error, DNL		-	-	$\pm 0.5$	LSB
<b>ANALOG INPUT</b>					
Analog Input Capacitance, $C_{IN}$	$V_{IN} = +3.0V$ , $+0.07V_{RMS}$	-	10	-	pF
Analog Input Resistance, $R_{IN}$		7	20	40	k $\Omega$
Analog Input Current, $I_{IN}$		0	100	285	$\mu\text{A}$

**Electrical Specifications**  $DV_{CC1, 2}, AV_{CC}, DGND3 = +5V, DGND1, 2, AGND, DV_{EE3} = 0V, V_{RT} = 4V, V_{RB} = 2V, T_A = 25^{\circ}C$  (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>REFERENCE INPUT</b>					
Reference Resistance (Note 3), $R_{REF}$		400	600	740	$\Omega$
Reference Current (Note 4), $I_{REF}$		2.7	3.3	5.0	mA
Offset Voltage $V_{RT}$ Side, EOT		6	8	10	mV
Offset Voltage $V_{RB}$ Side, EOB		0	1.5	3	mV
<b>DIGITAL INPUT (PECL/ECL)</b>					
Digital Input Voltage: High, $V_{IH}$		$DV_{EE3} + 1.5$	-	DGND3	V
Digital Input Voltage: Low, $V_{IL}$		$DV_{EE3} + 1.1$	-	$V_{IH} - 0.4$	V
Threshold Voltage, $V_{TH}$		-	DGND3 - 1.2	-	V
Digital Input Current: High, $I_{IH}$	$V_{IH} = DGND3 - 0.8V$	-50	-	+50	$\mu A$
Digital Input Current: Low, $I_{IL}$	$V_{IL} = DGND3 - 1.6V$	-50	-	0	$\mu A$
Digital Input Capacitance		-	-	5	pF
<b>DIGITAL INPUT (TTL)</b>					
Digital Input Voltage: High, $V_{IH}$		2.0	-	-	V
Digital Input Voltage: Low, $V_{IL}$		-	-	0.8	V
Threshold Voltage, $V_{TH}$		-	1.5	-	V
Digital Input Current: High, $I_{IH}$	$V_{IH} = 3.5V$	-10	-	0	$\mu A$
Digital Input Current: Low, $I_{IL}$	$V_{IL} = 0.2V$	-20	-	0	$\mu A$
Digital Input Capacitance		-	-	5	pF
<b>DIGITAL OUTPUT (TTL)</b>					
Digital Output Voltage: High, $V_{OH}$	$I_{OH} = -2mA$	2.4	-	-	V
Digital Output Voltage: Low, $V_{OL}$	$I_{OL} = 1mA$	-	-	0.5	V
<b>SWITCHING CHARACTERISTICS</b>					
Maximum Conversion Rate, $f_C$	DMUX Mode	120	-	-	MSPS
Aperture Jitter, $t_{AJ}$		-	10	-	ps
Sampling Delay, $t_{DS}$		1.2	1.4	1.6	ns
Clock High Pulse Width, $t_{PW1}$	CLK	3.0	-	-	ns
Clock Low Pulse Width, $t_{PW0}$	CLK	4.5	-	-	ns
RESET Signal Setup Time, $t_{RS}$	RESETN-CLK	1.0	-	-	ns
RESET Signal Hold Time, $t_{RH}$	RESETN-CLK	-0.5	-	-	ns
CLKOUT Output Delay, $t_{DCLK}$	$C_L = 5pF$	3.0	4.5	7.0	ns
Data Output Delay (Note 5), $t_{DO1}$ $t_{DO2}$	DEMUX Mode ( $C_L = 5pF$ )	-	$t + 0.5$	-	ns
	( $C_L = 5pF$ )	3.5	5.0	7.0	ns
Output Rise Time, $t_r$	0.8 to 2.0V ( $C_L = 5pF$ )	-	1	-	ns
Output Fall Time, $t_f$	0.8 to 2.0V ( $C_L = 5pF$ )	-	1	-	ns
<b>DYNAMIC CHARACTERISTICS</b>					
Input Bandwidth	$V_{IN} = 2V_{P-P}, -3dB$	250	-	-	MHz
S/N Ratio	$f_C = 120MSPS, f_{IN} = 1kHz$ Full Scale, DMUX Mode	-	46	-	dB
	$f_C = 120MSPS, f_{IN} = 29.999MHz$ Full Scale, DMUX Mode	-	42	-	dB
Error Rate (Note 6)	$f_C = 120MSPS, f_{IN} = 1kHz$ Full Scale, DMUX Mode, Error > 16 LSB	-	-	$10^{-12}$	TPS
	$f_C = 120MSPS, f_{IN} = 29.999MHz$ Full Scale, DMUX Mode, Error > 16 LSB	-	-	$10^{-9}$	TPS
	$f_C = 100MSPS, f_{IN} = 24.999MHz$ Full Scale, Straight Mode, Error > 16 LSB	-	-	$10^{-9}$	TPS
<b>POWER SUPPLY OPERATING (PS = 1)</b>					
Total Supply Current, $I_{CC} + I_{EE}$		70	98	140	mA

**Electrical Specifications**  $DV_{CC1, 2}, AV_{CC}, DGND3 = +5V, DGND1, 2, AGND, DV_{EE3} = 0V, V_{RT} = 4V, V_{RB} = 2V, T_A = 25^{\circ}C$  (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$AV_{CC}$ Pin Supply Current, $I_{CC}$		45	-	87	mA
$DV_{CC1}$ Pin Supply Current, $DICCC1$		20	-	36	mA
$DV_{CC2}$ Pin Supply Current, $DICCC2$		5	-	15	mA
$DGND3$ Pin Supply Current, $I_{EE}$		0.5	-	1.5	mA
Power Consumption, $PD^{*6}$		400	500	700	mW
<b>POWER SUPPLY IN POWER SAVING MODE (PS = 0)</b>					
Total Supply Current, PS $I_{CC} + I_{EE}$		-	-	5	mA
$AV_{CC}$ Pin Supply Current, PS $I_{CC}$		-	-	1.5	mA
$DV_{CC1}$ Pin Supply Current, PS $DICCC1$		-	-	1.5	mA
$DV_{CC2}$ Pin Supply Current, PS $DICCC2$		-	-	1.5	mA
$DGND3$ Pin Supply Current, PS $I_{EE}$		-	-	0.5	mA
Power Consumption, PS $PD^{*6}$		-	-	25	mW

NOTES:

3.  $R_{REF}$ : Resistance value between  $V_{RT}$  and  $V_{RB}$ .

$$4. I_{REF} = \frac{V_{RT} - V_{RB}}{R_{REF}}$$

$$5. t = \frac{1}{f_C}$$

6. The unit of measure TPS: Times Per Sample.

$$7. P_D = (I_{CC} + I_{EE}) \cdot V_{CC} + \frac{(V_{RT} - V_{RB})^2}{V_{REF}}$$

**Timing Diagrams**

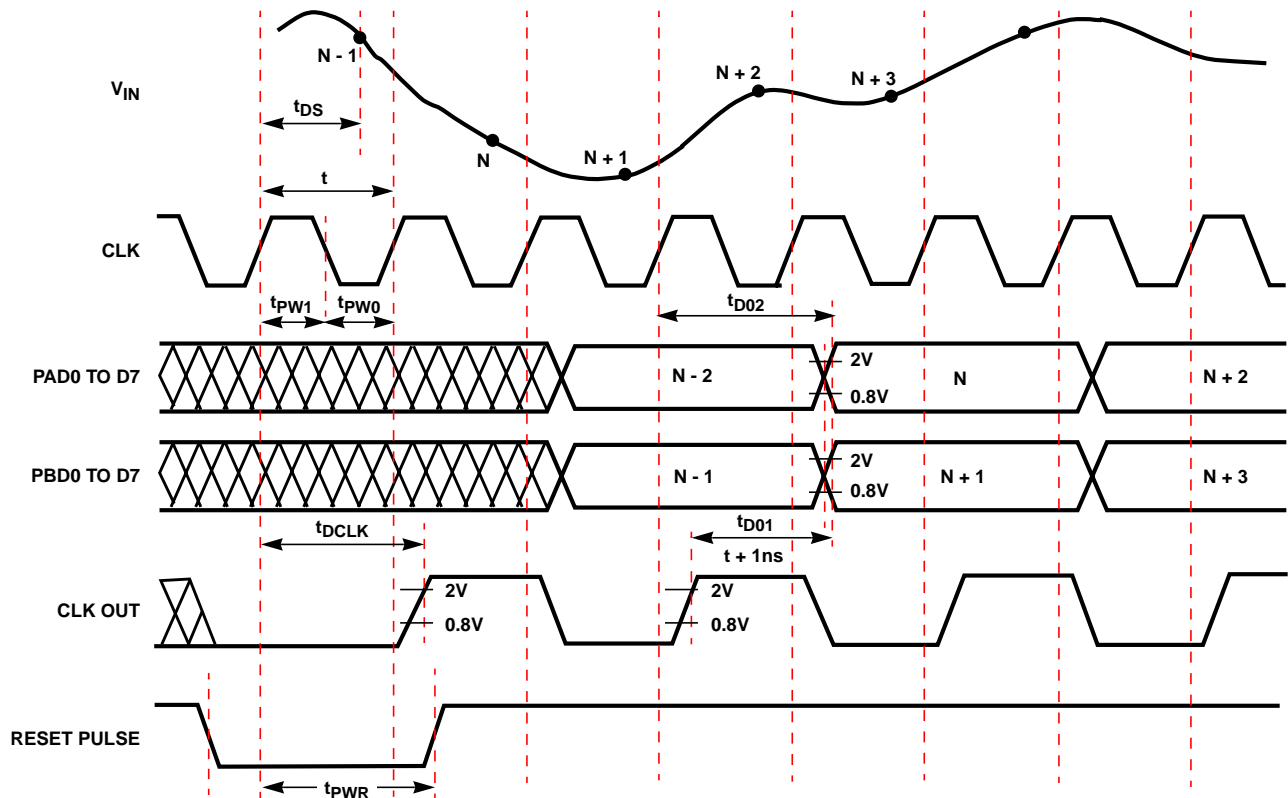


FIGURE 1. DEMUX MODE TIMING CHART (SELECT1 =  $V_{CC}$ )

Timing Diagrams (Continued)

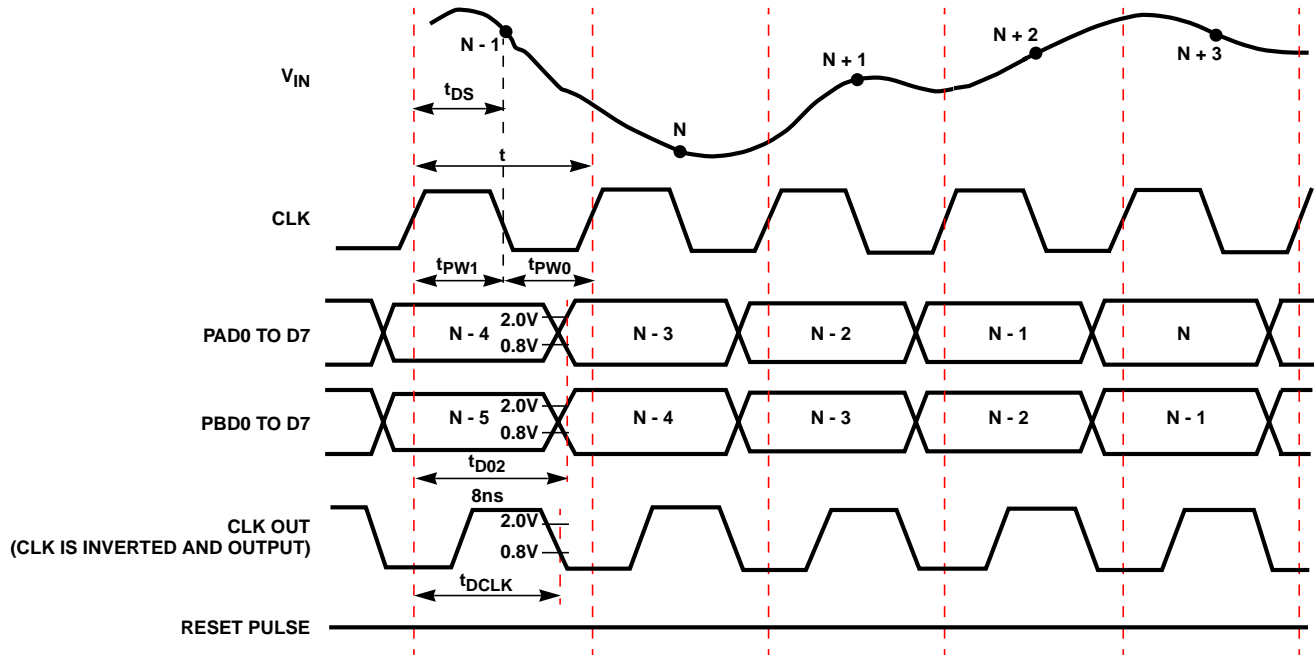


FIGURE 2. STRAIGHT MODE TIMING CHART (SELECT1 = GND)

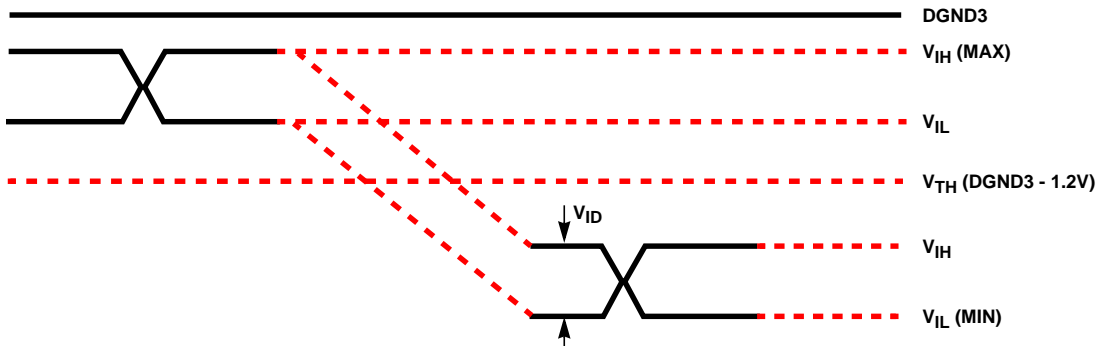


FIGURE 3. PECL SWITCHING LEVEL

Pin Descriptions

PIN NO	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
3, 10	AGND		GND		Analog Ground. Separated from the digital ground.
5, 8	AV <sub>CC</sub>		+5V (Typ)		Analog Power Supply. Separated from the digital power supply.
20, 29 32, 41	DGND1 DGND2		GND		Digital Ground.
19, 30 31, 42	DV <sub>CC</sub> 1 DV <sub>CC</sub> 2		+5V (Typ)		Digital Power Supply.
12	DGND3		+5V (Typ) (With a Single Power Supply) GND (With Dual Power Supplies)		Digital Power Supply. Apply -5V for PECL and TTL input.
1	DV <sub>EE</sub> 3		GND (With a Single Power Supply) +5V (Typ) (With Dual Power Supplies)		Digital Power Supply. Apply -5V for PECL and TTL input.

**Pin Descriptions** (Continued)

PIN NO	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
16	SELECT2	I	DV <sub>CC1</sub> , DGND1 or Open		Data output switching. Data is output from both PA and PD when left open. If pin is connected to DV <sub>CC1</sub> , only PA is used as output with PB high impedance. If pin is connected to DGND1, only PB is used as output with PA high impedance.
17	VOCLP	I	Clamp Voltage		Defines TTL output high level. If left open the high level is ~ 2.8V.
18	PS	I	TTL		Power Savings pin. When left open or at high level the device operates normally. When set to low level the power saving mode enabled.
13	CLK/E	I	PECL/ECL		Clock Input.
14	CLK/NE	I			CLK/E Complementary Input. When left open, this pin goes to the threshold potential. Only CLK/E can be used for operation, but complementary input is recommended to attain fast and stable operation.
48	RESETN/E	I			Reset Input. When the input is set to low level, the built-in CLK frequency divider circuit can be reset.
47	RESET/E	I			RESETN/E Complementary Input. When left open, this pin goes to the threshold voltage. Only RESETN/E can be used for operation.
15	CLK/T	I	TTL		Clock input.
46	RESETN/T	I			Reset Input. When left open, this input goes to high level. When the input is set to low level, the built-in CLK frequency divider circuit can be reset.
44	INV	I	TTL		Data Output Polarity Inversion Input. When left open, this input goes to high level. (See Table 1; I/O Correspondence Table).

Pin Descriptions (Continued)

PIN NO	SYMBOL	I/O	TYPICAL VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
45	SELECT1		V <sub>CC</sub> or Ground		Data Output Mode Selection. (See Table 2; Operating Mode Table).
11	V <sub>RT</sub>	I	4.0V (Typ)		Top Reference Voltage. Bypass to AGND with a 1μF tantal capacitor and a 0.1μF chip capacitor.
9	V <sub>RM3</sub>		$V_{RB} + \frac{3}{4} (V_{RT} - V_{RB})$		Reference Voltage Mid Point. Bypass to AGND with a 0.1μF chip capacitor.
7	V <sub>RM2</sub>		$V_{RB} + \frac{2}{4} (V_{RT} - V_{RB})$		Reference Voltage Mid Point. Bypass to AGND with a 0.1μF chip capacitor.
4	V <sub>RM1</sub>		$V_{RB} + \frac{1}{4} (V_{RT} - V_{RB})$		Reference Voltage Mid Point. Bypass to AGND with a 0.1μF chip capacitor.
2	V <sub>RB</sub>	I	2.0V (Typ)		Bottom Reference Voltage. Bypass to AGND with a 1μF tantal capacitor and a 0.1μF chip capacitor.
6	V <sub>IN</sub>	I	V <sub>RT</sub> to V <sub>RB</sub>		Analog Input.
33 to 40	PBD0 to PBD7	O	TTL		Port 1 Side Data Output.
21 to 28	PAD0 to PAD7	O			Port 2 Side Data Output.
43	CLKOUT	O			Clock Output. (See Table 2; Operating Mode Table).



TABLE 1. A/D CODE

V <sub>IN</sub>	STEP	INV															
		1				0											
		D7	D6	D5	D0	D7	D6	D5	D0								
V <sub>RT</sub>	255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	254	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1
	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
V <sub>RM2</sub>	128	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	127	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
V <sub>RB</sub>	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

**Notes on Operation**

- The HI3256 is a high-speed A/D converter which is capable of TTL, ECL and PECL level clock input. Characteristic impedance should be properly matched to ensure optimum performance during high-speed operation.
- The power supply and grounding have a profound influence on converter performance. The power supply and grounding method are particularly important during high-speed operation. General points for caution are as follows:
  - The ground pattern should be as large as possible. It is recommended to make the power supply and ground patterns wider at an inner layer using a multi-layer board.

- To prevent interference between AGND and DGND and between AV<sub>CC</sub> and DV<sub>CC</sub>, make sure the respective patterns are separated. To prevent a DC offset in the power supply pattern, connect the AV<sub>CC</sub> and DV<sub>CC</sub> lines at one point each, via a ferrite-bead filter. Shorting the AGND and DGND patterns in one place immediately under the A/D converter improves A/D converter performance.
- Ground the power supply pins (AV<sub>CC</sub>, DV<sub>CC1</sub>, DV<sub>CC2</sub>, DV<sub>EE3</sub>) as close to each pin as possible with a 0.1μF or larger ceramic chip capacitor. (Connect the AV<sub>CC</sub> pin to the AGND pattern and the DV<sub>CC1</sub>, DV<sub>CC2</sub>, DV<sub>EE3</sub> pins to the DGND pattern).
- The digital output wiring should be as short as possible. If the digital output wiring is long, the wiring capacitance will increase, deteriorating the output slew rate and resulting in reflection to the output waveform since the original output slew rate is quite fast.
- The analog input pin V<sub>IN</sub> has an input capacitance of approximately 21pF. To drive the A/D converter with proper frequency response, it is necessary to prevent performance deterioration due to parasitic capacitance or parasitic inductance by using a large capacity drive circuit; keeping wiring as short as possible, and using chip parts for resistors and capacitors, etc.
- The V<sub>RT</sub> and V<sub>RB</sub> pins must have adequate bypass to protect them from high-frequency noise. Bypass them to AGND with approximately 1μF tantal capacitor and, 0.1μF capacitor. At this time, approximately DGND3 - 1.2V voltage is generated. However, this is not recommended for use as threshold voltage V<sub>BB</sub> as it is too weak.

When the digital input level is PECL level, \*\*\*/E pins should be used and \*\*\*/T pins left open. When the digital input level is TTL, \*\*\*/T pins should be used and III/E pins left open.

**Test Circuits**

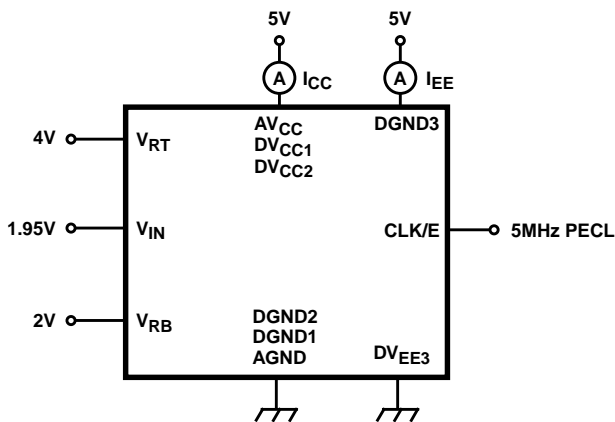


FIGURE 4. CURRENT CONSUMPTION MEASUREMENT CIRCUIT

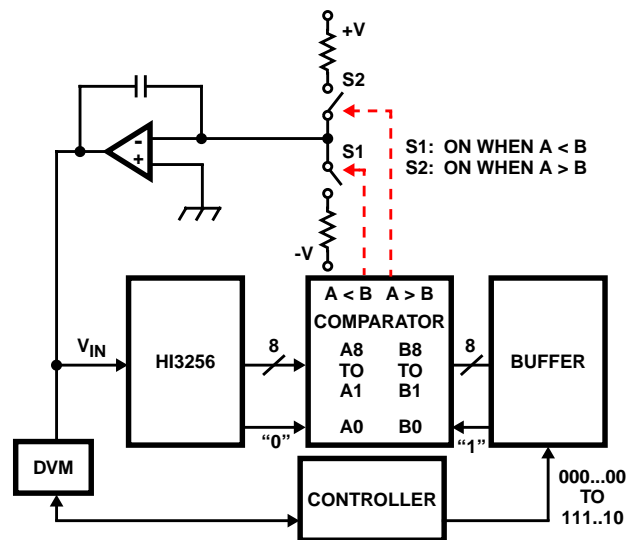


FIGURE 5. INTEGRAL LINEARITY ERROR/DIFFERENTIAL LINEARITY ERROR MEASUREMENT CIRCUIT

**Test Circuits** (Continued)

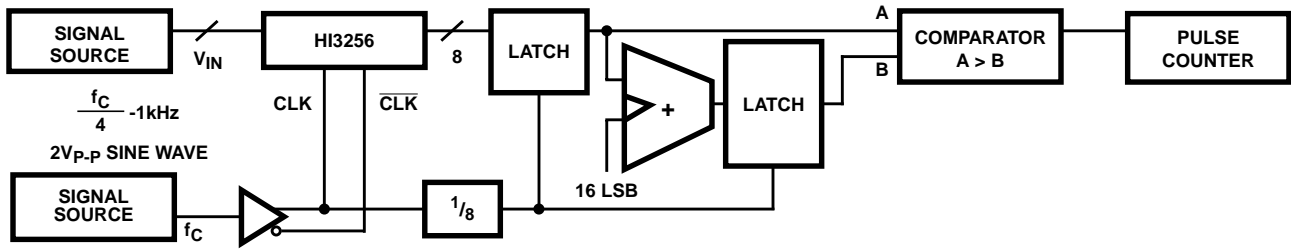


FIGURE 6. ERROR RATE MEASUREMENT CIRCUIT

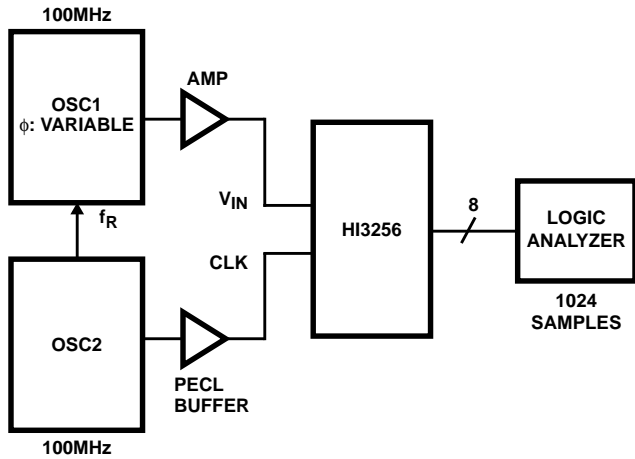
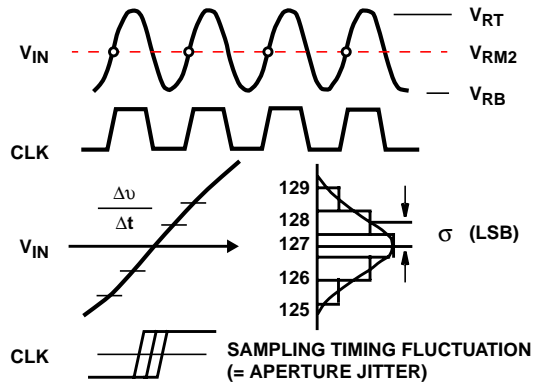


FIGURE 7. SAMPLING DELAY/APERTURE JITTER MEASUREMENT CIRCUIT



NOTE: Where  $\sigma$  (LSB) is the deviation of the output codes when the largest slew rate point is sampled at the clock which has exactly the same frequency as the analog input signal, the aperture jitter  $t_{AJ}$  is:

$$t_{AJ} = \left( \sigma \frac{\Delta v}{\Delta t} \right) = \sigma / \left( \frac{256}{2} \times 2\pi f \right).$$

FIGURE 8. APERTURE JITTER MEASUREMENT METHOD

**Operating Modes**

The HI3256 has two types of operating modes which are selected with Pin 45 (SELECT1).

TABLE 2. OPERATING MODE

OPERATING MODE	SELECT1	MAXIMUM CONVERSION RATE	DATA OUTPUT	CLOCK OUTPUT
DMUX Mode	V <sub>CC</sub>	120MSPS	Demultiplexed Output 60MBPS	The input clock is $1/2$ frequency divided and output at 60MHz.
Straight Mode	GND	100MSPS	Straight Output 100MBPS	The input clock is inverted and output at 100MHz.

**DMUX Mode (See Application Circuits, Figures 18, 19)**

Set the SELECT1 pin to V<sub>CC</sub> for this mode. In this mode, the clock frequency is divided by 2 in the IC, and the data is output after being demultiplexed by this  $1/2$  frequency divided clock. The  $1/2$  frequency divided clock, which has adequate setup time and hold time for the output data, is output from the CLKOUT pin.

When using multiple HI3256 units in parallel in this mode, differences in the start timing of the  $1/2$  frequency divided clock may cause operation as shown in Figure 9. As a countermeasure, the HI3256 is equipped with a function which resets the  $1/2$  frequency divided clock. When resetting this clock, the RESET pulse must be input to the RESET pin. See the Timing Charts for the RESET pulse input timing. The A/D converter can operate at  $f_C$  (Min) = 120MSPS in this mode.

**Straight Mode (See Application Circuits, Figures 20, 21)**

Set the SELECT1 pin to GND for this mode. In this mode, data output can be obtained in accordance with the clock frequency applied to the A/D converter for applications which use the clock applied to the A/D converter as the system clock. The A/D converter can operate at  $f_C$  (Min) = 100MSPS in this mode.

**Digital Input Level and Supply Voltage Settings**

The logic input level for the HI3256 supports PECL and TTL levels.

The power supplies (DV<sub>EE3</sub>, DGND3) for the logic input block must be set to match the logic input (CLK and RESET signals) level.

TABLE 3. LOGIC INPUT LEVEL AND POWER SUPPLY SETTINGS

DIGITAL INPUT LEVEL	DVEE3	DGND3	SUPPLY VOLTAGE	APPLICATION CIRCUITS
PECL	0V	+5V	+5V	Figures 18, 20
TTL	0V	+5V	+5V	Figures 19, 21

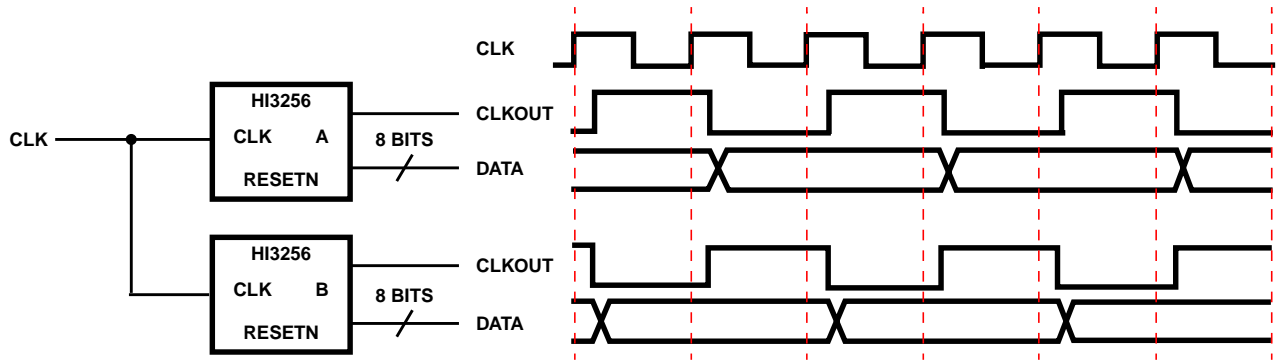


FIGURE 9. WHEN THE RESET PULSE IS NOT USED

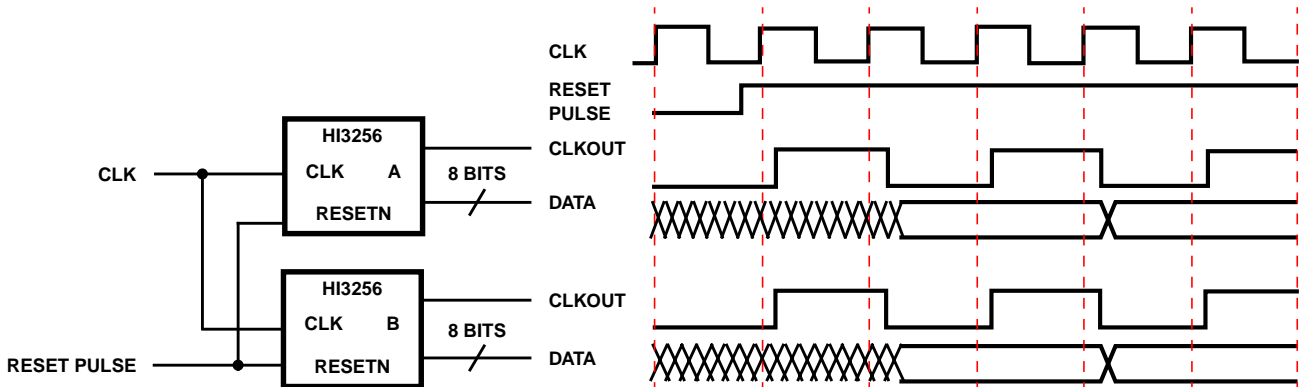


FIGURE 10. WHEN THE RESET PULSE IS USED

Typical Performance Curves

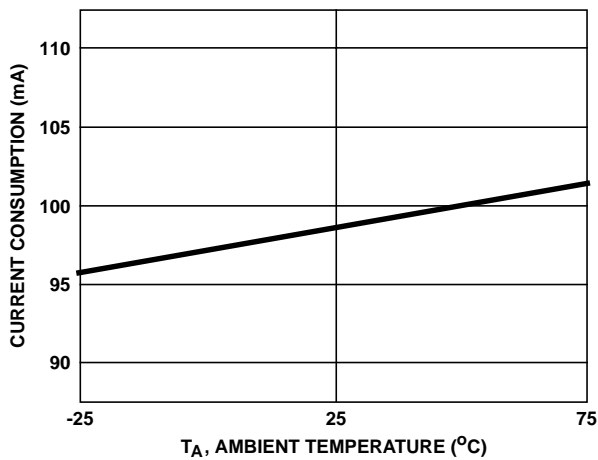


FIGURE 11. CURRENT CONSUMPTION vs AMBIENT TEMPERATURE CHARACTERISTICS

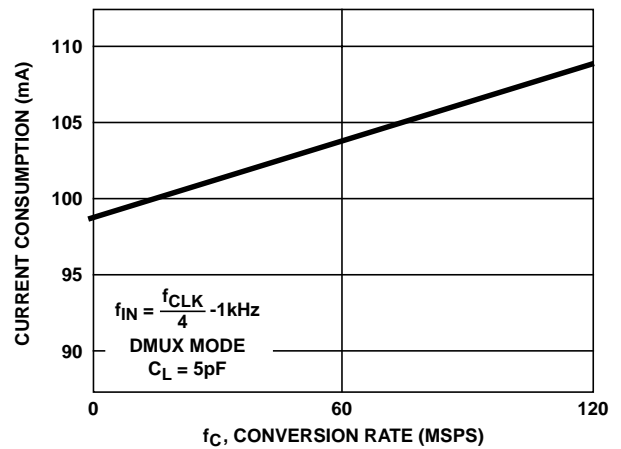


FIGURE 12. CURRENT CONSUMPTION vs CONVERSION RATE CHARACTERISTICS RESPONSE

Typical Performance Curves (Continued)

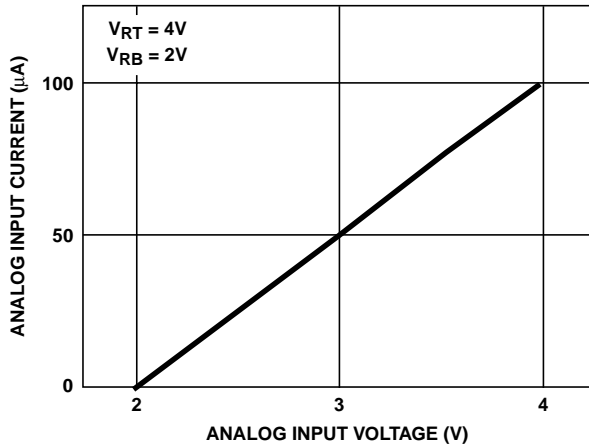


FIGURE 13. ANALOG INPUT CURRENT vs ANALOG INPUT VOLTAGE CHARACTERISTICS

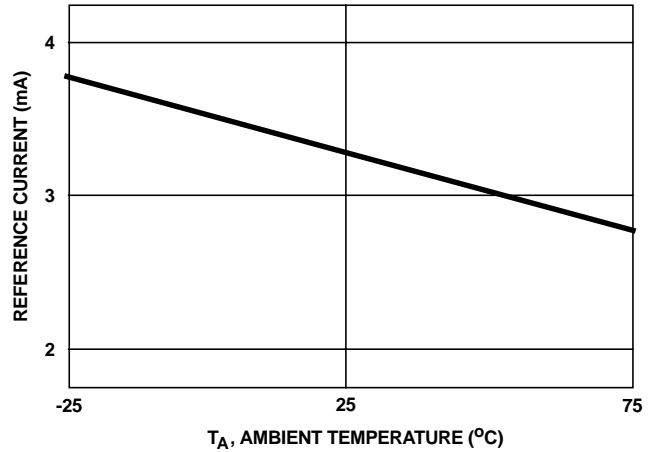


FIGURE 14. REFERENCE CURRENT vs AMBIENT TEMPERATURE CHARACTERISTICS

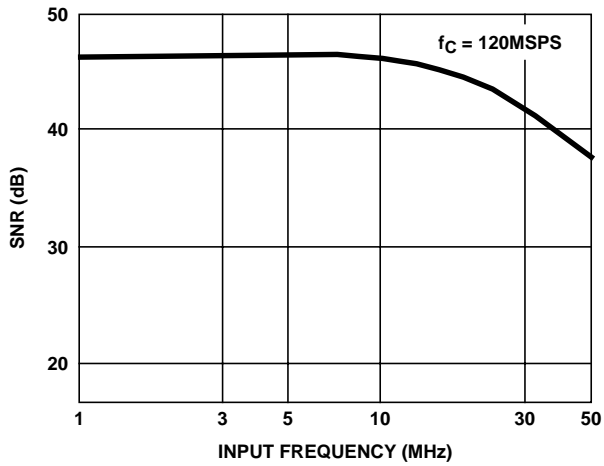


FIGURE 15. SNR vs INPUT FREQUENCY RESPONSE

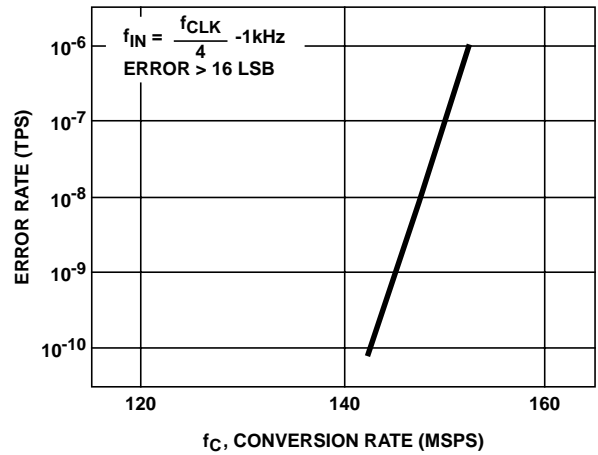


FIGURE 16. ERROR RATE vs CONVERSION RATE CHARACTERISTICS

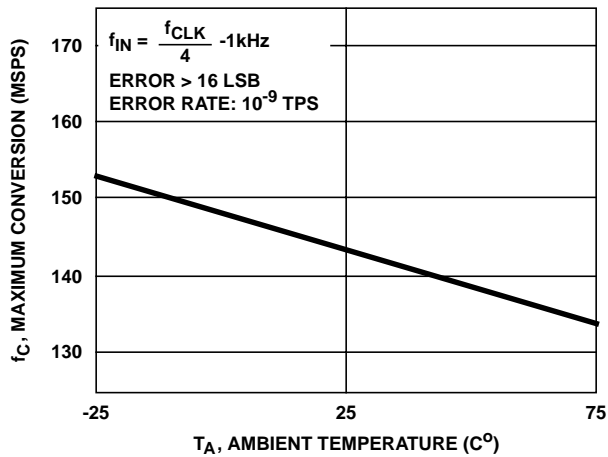


FIGURE 17. MAXIMUM CONVERSION RATE vs AMBIENT TEMPERATURE CHARACTERISTICS

Application Circuits

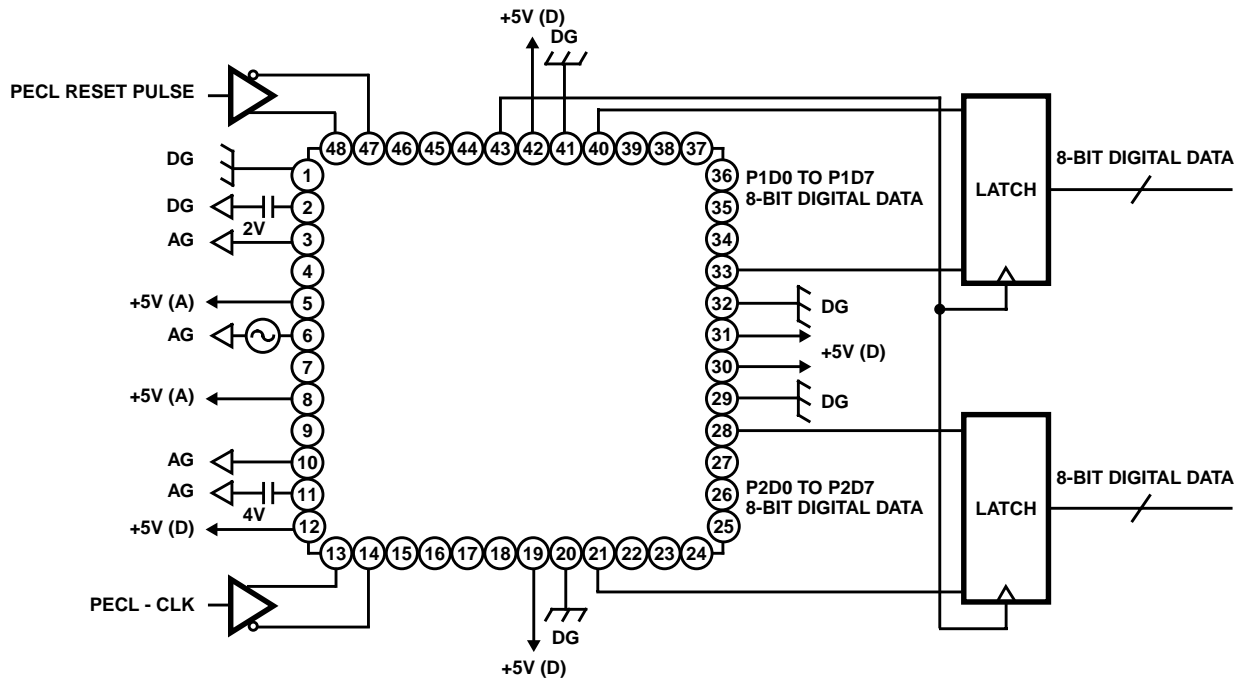


FIGURE 18. DMUX PECL INPUT

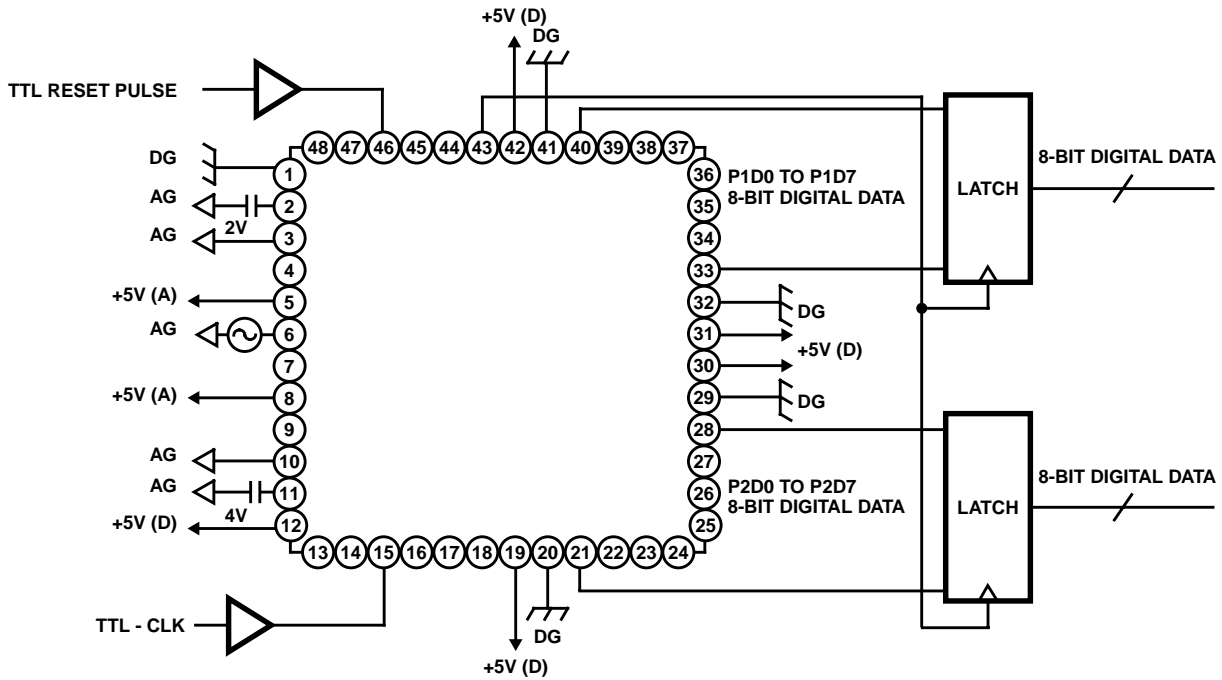


FIGURE 19. DMUX TTL INPUT

Application Circuits (Continued)

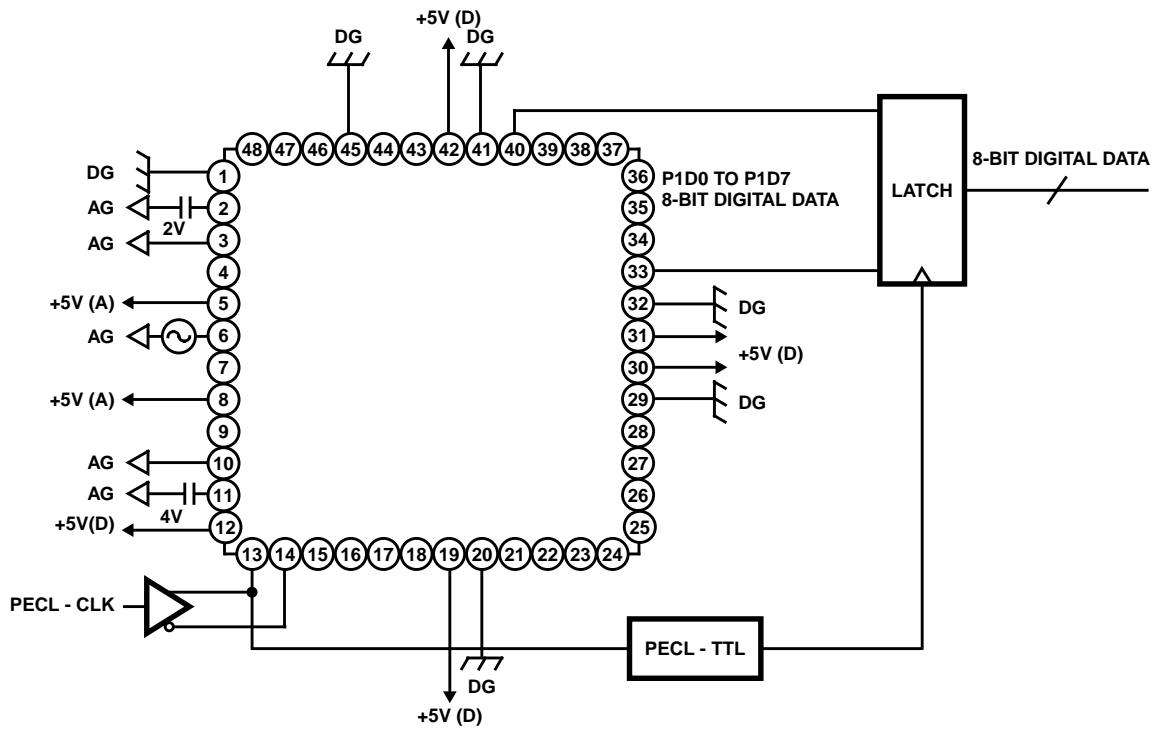


FIGURE 20. STRAIGHT PECL INPUT

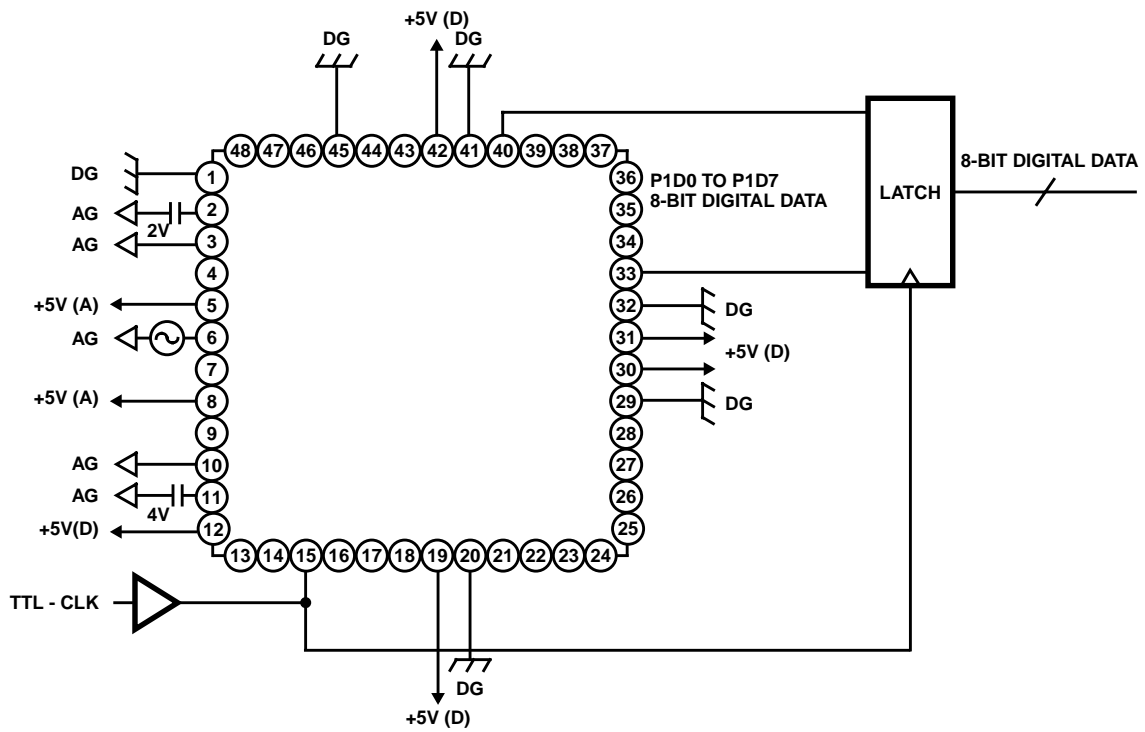


FIGURE 21. STRAIGHT TTL INPUT

Application Circuits (Continued)

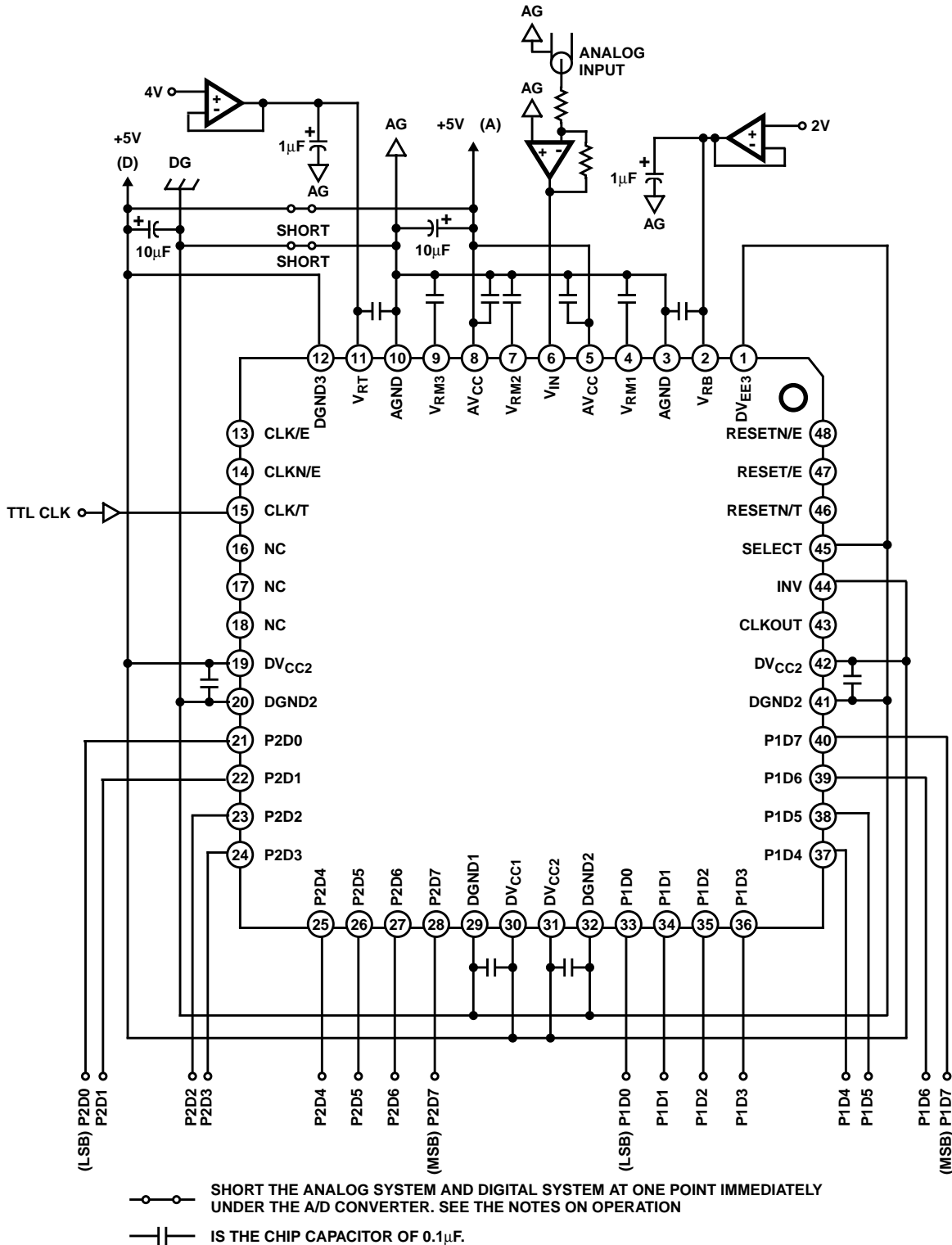
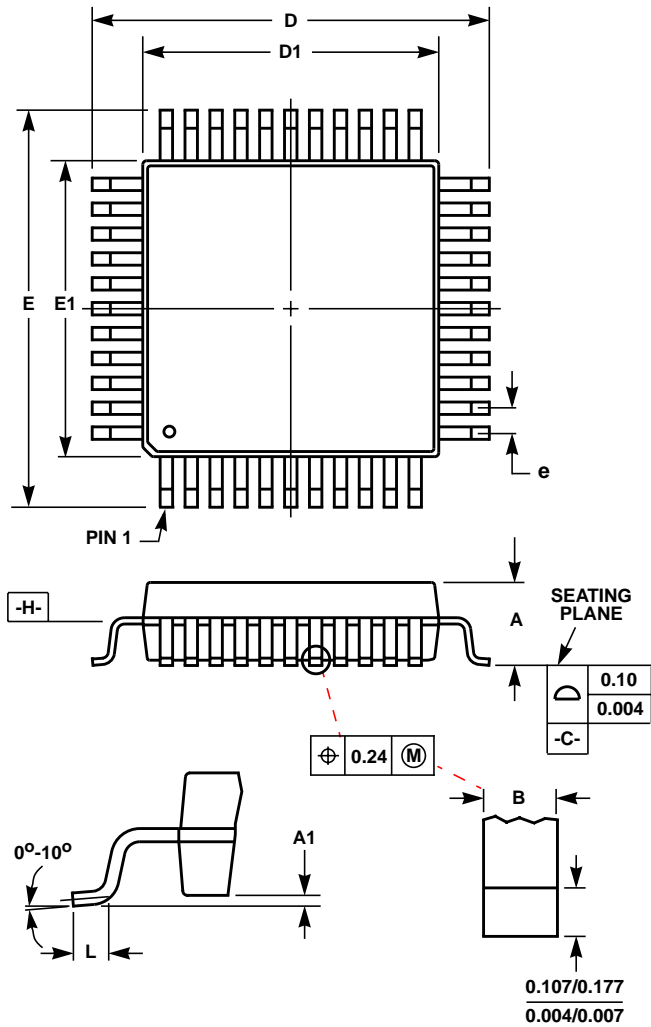


FIGURE 22. STRAIGHT MODE TTL I/O (WHEN A SINGLE POWER SUPPLY IS USED)

**Metric Plastic Quad Flatpack Packages (MQFP/PQFP)**



**Q48.7x7-S**

**48 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.056	0.066	1.40	1.70	-
A1	0.000	0.007	0.00	0.20	-
B	0.006	0.010	0.15	0.26	5
D	0.347	0.362	8.80	9.20	2
D1	0.272	0.279	6.90	7.10	3, 4
E	0.347	0.362	8.80	9.20	2
E1	0.272	0.279	6.90	7.10	3, 4
L	0.012	0.027	0.30	0.70	-
N	48		48		6
e	0.020 BSC		0.500 BSC		-

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**NOTES:**

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. Dimensions D and E to be determined at seating plane -C-.
3. Dimensions D1 and E1 to be determined at datum plane -H-.
4. Dimensions D1 and E1 do not include mold protrusion.
5. Dimension B does not include dambar protrusion.
6. "N" is the number of terminal positions.

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**Sales Office Headquarters**

**NORTH AMERICA**

Intersil Corporation  
 P. O. Box 883, Mail Stop 53-204  
 Melbourne, FL 32902  
 TEL: ( ) 724-7000  
 FAX: ( ) 724-7240

**EUROPE**

Intersil SA  
 Mercure Center  
 100, Rue de la Fusee  
 1130 Brussels, Belgium  
 TEL: (32) 2.724.2111  
 FAX: (32) 2.724.22.05

**ASIA**

Intersil (Taiwan) Ltd.  
 7F-6, No. 101 Fu Hsing North Road  
 Taipei, Taiwan  
 Republic of China  
 TEL: (886) 2 2716 9310  
 FAX: (886) 2 2715 3029