Data Sheet | January 1999 | File Number 4643

NTSC/PAL Video Decoder

The HMP8117 is a high quality NTSC and PAL video decoder with internal A/D converters. It is compatible with NTSC M, PAL B, D, G, H, I, M, N, and combination N (N_C) video standards.

Both composite and S-video (Y/C) input formats are supported. A 2-line comb filter plus a user-selectable chrominance trap filter provide high quality Y/C separation. User adjustments include brightness, contrast, saturation, hue, and sharpness.

Vertical blanking interval (VBI) data, such as Closed Captioning, Wide Screen Signalling and Teletext, may be captured and output as BT.656 ancillary data. Closed Captioning and Wide Screen Signalling information may also be read out via the I^2C interface.

The Videolyzer™ feature provides approved Macrovision™ copy-protection bypass and detection.

Ordering Information

PART NUMBER	TEMP RANGE (^oC)	PACKAGE	PACKAGE NO.
HMP8117CN	0 to 70	80 Ld PQFP	Q80.14x20
HMPVIDEVAL/ISA	Evaluation Board: ISA Frame Grabber		

NOTES:

1. PQFP is also known as QFP and MQFP.
2. Evaluation Board descriptions are in the Applications section.

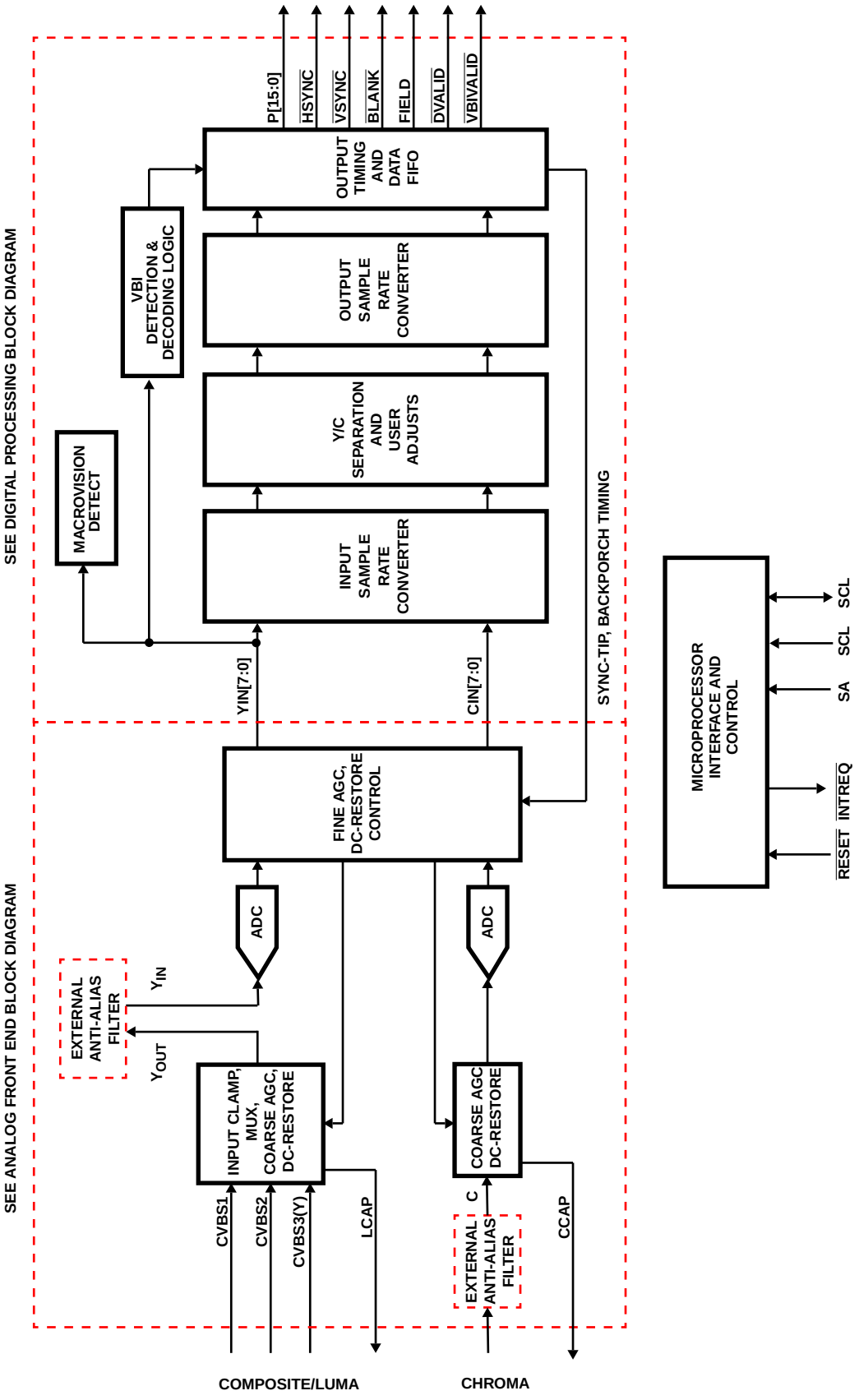
Features

- (M) NTSC and (B, D, G, H, I, M, N, N_C) PAL Operation
  - Optional Auto Detect of Video Standard
  - ITU-R BT.601 (CCIR601) and Square Pixel Operation
- Videolyzer Feature
  - Macrovision™ Bypass and Detection
- Digital Anti-Alias Filter
- Power Down Mode
- Digital Output Formats
  - VMI Compatible
  - 8-bit, 16-bit 4:2:2 YCbCr
  - 15-bit (5,5,5), 16-bit (5,6,5) RGB
  - Linear or Gamma-Corrected
  - 8-bit BT.656
- Analog Input Formats
  - Three Analog Composite Inputs
  - Analog Y/C (S-video) Input
- “Raw” (Oversampled) VBI Data Capture
- “Sliced” VBI Data Capture Capabilities
  - Closed Captioning
  - Widescreen Signalling (WSS)
  - BT.653 System B, C and D Teletext
  - North American Broadcast Teletext (NABTS)
  - World System Teletext (WST)
- 2-Line (1H) Comb Filter Y/C Separator
- Fast I^2C Interface

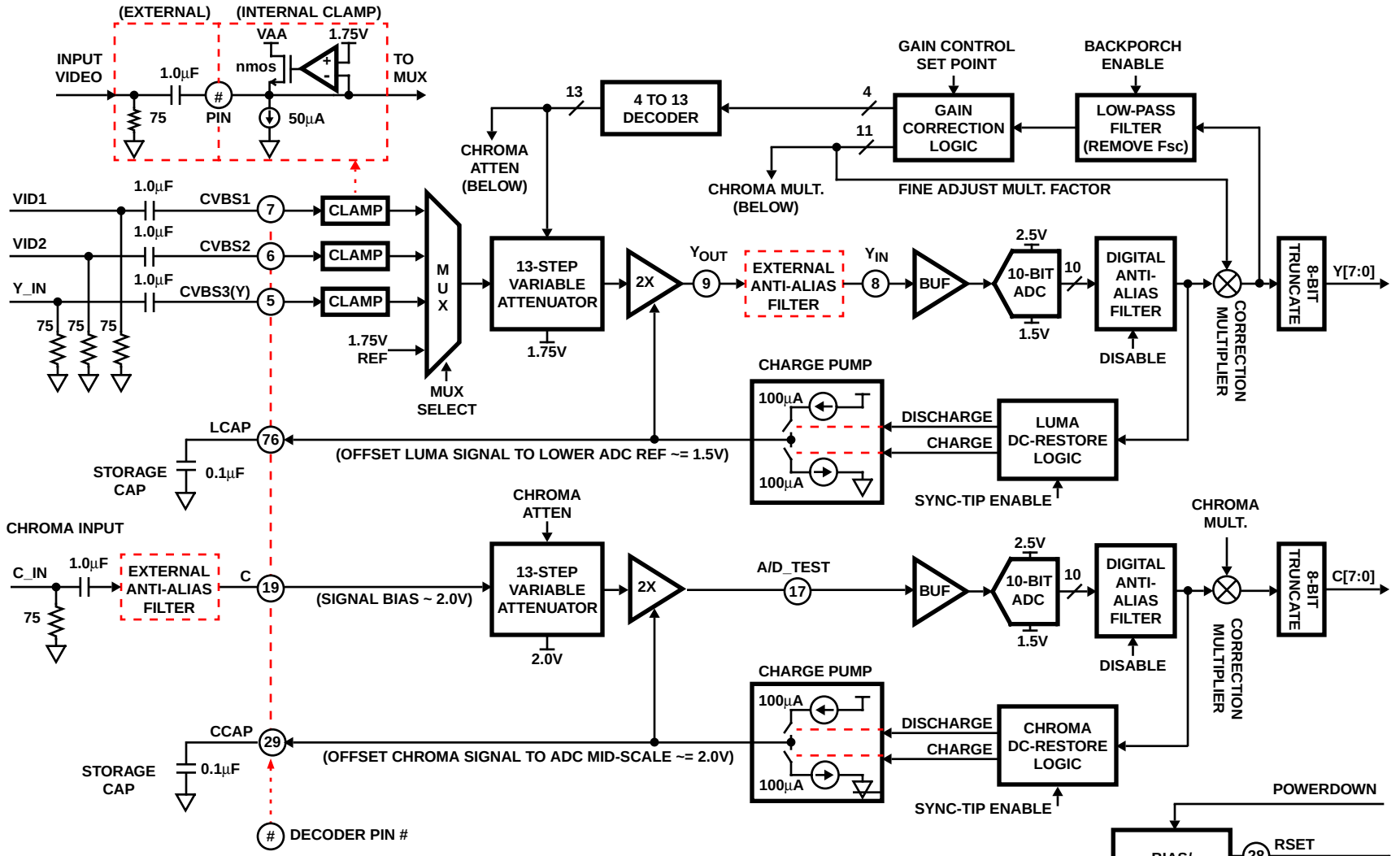
Applications

- Multimedia PCs
- Video Conferencing
- Video Compression Systems
- Video Security Systems
- LCD Projectors and Overhead Panels
- Related Products
  - NTSC/PAL Encoders: HMP815x, HMP817x, HMP819x
  - NTSC/PAL Decoders: HMP8112A, HMP8115

Functional Block Diagram



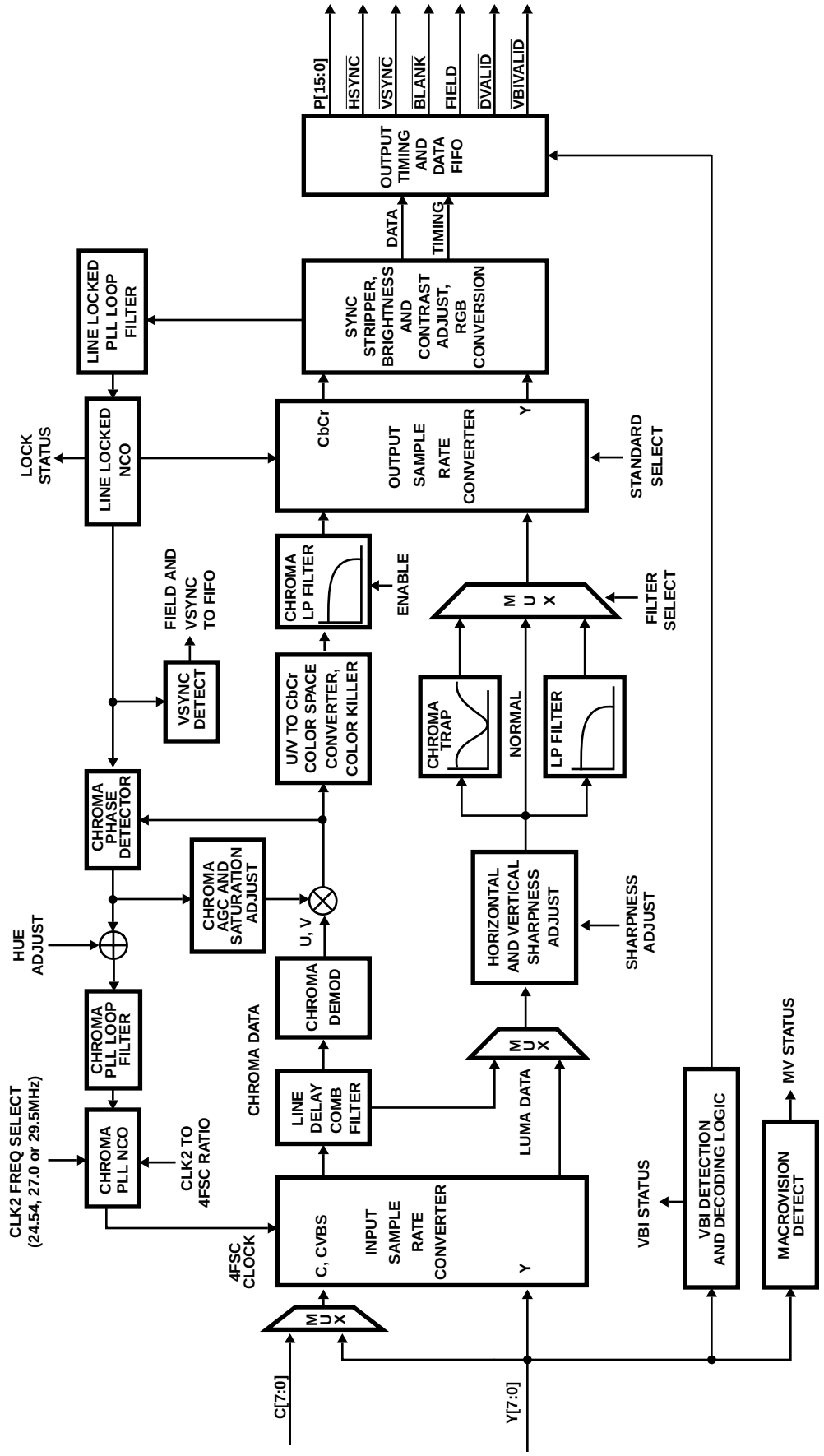
Analog Front End Block Diagram



PIN #	NOMINAL (NTSC) OPERATING CONDITION
5, 6, 7	CVBSX. SIZE = INPUT. SYNC TIP CLAMPED AT ~= 1.75 VDC.
9, 8	Y_{OUT}/Y_{IN}. SIZE = ~1.0 V_{P-P}, SYNC TIP OFFSET ~= 1.5 VDC.
19	C. SIZE = INPUT SIZE. PORCH OFFSET ~= 2.0 VDC.
17	A/D_TEST. SIZE ~= F(LUMA AGC), PORCH OFFSET ~= 2.0VDC.

PIN #	NOMINAL (NTSC) OPERATING CONDITION
76	LCAP. DC-SIGNAL OFFSET ~= 2.4 VDC.
29	CCAP. DC-SIGNAL OFFSET ~= 2.4 VDC.
28	RSET. DC-SIGNAL OFFSET ~= 1.2 VDC.
78	REF_CAP. DC-SIGNAL OFFSET ~= 2.5 VDC.

Digital Processing Block Diagram



Introduction

The HMP8117 is designed to decode baseband composite or S-video NTSC and PAL signals, and convert them to either digital YCbCr or RGB data. In addition to performing the basic decoding operations, these devices include hardware to decode different types of VBI data and to generate full-screen blue, black and color bar patterns.

Digital PLLs are used to synchronize to all NTSC and PAL standards. A chroma PLL is used to maintain color lock for chroma demodulation while a line-locked PLL is used to maintain vertical spatial alignment. The PLLs are designed to maintain lock in the presence of VCR head switches, VCR trick-mode and multi-path noise.

The HMP8117 provides the Videolyzer feature for Macrovision (MV) copy-protection bypass and detection.

External Video Processing

Before a video signal can be digitized the decoder has some external processing considerations that need to be addressed. This section discusses those external aspects of the HMP8117.

Analog Video Inputs

The HMP8117 supports either three composite or two composite and one S-video input.

Three analog video inputs (CVBS 1-3) are used to select which one of three composite video sources are to be decoded. To support S-video applications, the Y channel drives the CVBS3(Y) analog input, and the C channel drives the C analog input.

The analog inputs must be AC-coupled to the video signals, as shown in the Applications section.

Anti-alias Filters

Although a 23 tap digital halfband anti-alias filter is provided for each A/D channel, an external passive filter is recommended for optimum performance. The digital filter has a flat response out to 5.4MHz with an approximate -3dB bandwidth of 6.3MHz using a 27MHz input CLK2 sample rate. For the CVBSx inputs, the filter is connected between the YOUT and YIN pins. For the C (chroma) input, the anti-alias filter should be connected before the C input. Recommended filter configurations are shown on the reference schematic in Figure 20. These filters have flat response out to 4.2MHz with an approximate -3dB bandwidth of 8MHz. If upgrading from the HMP8115 or HMP8112A, the previous filter configurations may be used but with slightly degraded bandwidth. Alternative higher or lower performance filters configurations may substituted.

Digitization of Video

Prior to A/D conversion, the input signal is offset and scaled to known video levels. After digitization, sample rate converters and a comb filter are used to perform color separation and demodulation.

A/D Conversion

Each CVBSX video input channel has a video clamp circuit that is independent of PLL timing. The input clamp provides a coarse signal offset to position the sync tip within the A/D converter sampling range so that the AGC and DC-RESTORE logic can operate.

A/D Conversion

Video data is sampled at the CLK2 frequency then processed by the input sample rate converter. The output levels of the ADC after AGC and DC restoration processing are:

	(M) NTSC (M, N) PAL	(B, D, G, H, I, N_C) PAL
white	196	196
black	66	59
blank	56	59
sync	0	0

AGC and DC Restoration

The AGC amplifier attenuates or amplifies the analog video signal to ensure that the blank level generates code 56 or 59 depending on the video standard. The difference from the ideal blank level of 56 or 59 is used to control the amount of attenuation or gain of the analog video signal. To obtain a stable DC reference for the AGC, a digital low-pass filter removes the chroma burst from the input signal's backporch.

DC restoration positions the video signal so that the sync tip generates a code 0. The internal timing windows for AGC and DC restoration are show in Figure 3. The appropriate windows are automatically determined by the decoder when the input signal is auto-detected or manually selected.

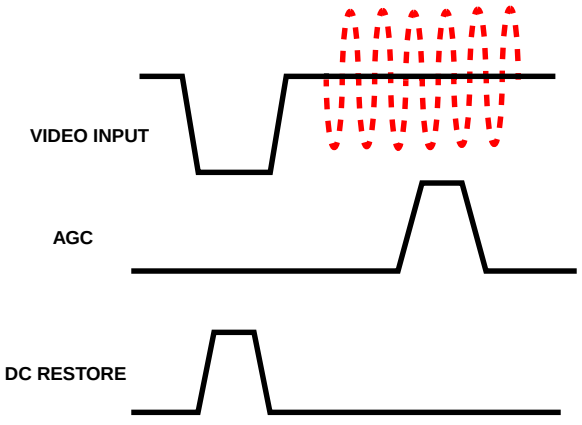


FIGURE 1. AGC AND DC RESTORE INTERNAL TIMING

Input Signal Detection

If no input video signal is detected for 16 consecutive line periods, nominal video timing is generated for the previously detected or programmed video standard. A maskable interrupt is provided for the condition of “Input Signal Loss” allowing the host to enable blue field output if desired.

Vertical Sync and Field Detection

The vertical sync and field detect circuit uses a low time counter to detect the vertical sync sequence in the video data stream. The low time counter accumulates the low time encountered during any sync pulse, including serration and equalization pulses. When the low time count exceeds the vertical sync detect threshold, $\overline{\text{VSYNC}}$ is asserted immediately. FIELD is asserted at the same time that $\overline{\text{VSYNC}}$ is asserted. FIELD is asserted low for odd fields and high for even fields. Field is determined from the location in the video line where VSYNC is detected. If VSYNC is detected in the first half of the line, the field is odd. If VSYNC is detected in the second half of a line, the field is even.

In the case of lost vertical sync or excessive noise that would prevent the detection of vertical sync, the FIELD output will continue to toggle. Lost vertical sync is declared if after 337 lines, a vertical sync period was not detected for 1 or 3 (selectable) successive fields as specified by bit 2 of the GENLOCK CONTROL register 04_H. When this occurs, the PLLs are initialized to the acquisition state.

Y/C Separation

A composite video signal has the luma (Y) and chroma (C) information mixed in the same video signal. The Y/C separation process is responsible for separating the composite video signal into these two components. The HMP8117 utilizes a comb filter to minimize the artifacts that are associated with the Y/C separation process.

Input Sample Rate Converter

The input sample rate converter is used to convert video data sampled at the CLK2 rate to a virtual $4xf_{SC}$ sample rate for comb filtering and color demodulation. An interpolating filter is used to generate the $4xf_{SC}$ samples as illustrated in Figure 2.

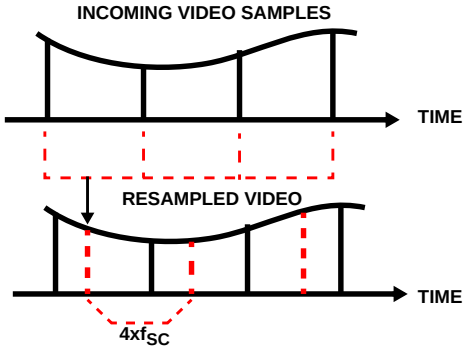


FIGURE 2. SAMPLE RATE CONVERSION

Comb Filter

A 2-line comb filter, using a single line delay, is used to perform part of the Y/C separation process. During S-video operation, the Y signal bypasses the comb filter; the C signal is processed by the comb filter since it is an integral part of the chroma demodulator. During PAL operation, the chroma trap filter should also be enabled for improved performance.

Since a single line store is used, the chroma will normally have a half-line vertical offset from the luma data. This may be eliminated, vertically aligning the chroma and luma samples, at the expense of vertical resolution of the luma. Bit 0 of the OUTPUT FORMAT register 02_H controls this option.

Chroma Demodulation

The output of the comb filter is further processed using a patented frequency domain transform to complete the Y/C separation and demodulate the chrominance.

Demodulation is done at a virtual $4xf_{SC}$ sample rate using the interpolated data samples to generate U and V data. The demodulation process decimates by 2 the U/V sample rate.

Output Sample Rate Converter

The output sample rate converter converts the Y, U and V data from a virtual $4xf_{SC}$ sample rate to the desired output sample rate (i.e., 13.5MHz). It also vertically aligns the samples based on the horizontal sync information embedded in the digital video data stream. The output sample rate is determined by the input video standard and the selected rectangular/square pixel mode. The output pixel rate is 1/2 of the CLK2 input clock frequency. The output format is 4:2:2 for all modes except the RGB modes which use a 4:4:4 output format.

CLK2 Input

The decoder requires a stable clock source for the CLK2 input. For best performance, use termination resistor(s) to minimize pulse overshoot and reflections on the CLK2 input. Since chroma demodulation uses the virtual $4xf_{SC}$, any jitter on CLK2 will be transferred as chrominance error on the output pixels. The CLK2 clock frequency must be one of the valid selections from Table 1 below based on the video standard and desired pixel mode.

TABLE 1. VIDEO STANDARD CLOCK RATE SELECTION SUMMARY

VIDEO FORMAT	VALID CLK2 FREQUENCIES (MHz)	
	RECTANGULAR PIXEL MODE	SQUARE PIXEL MODE
(M) NTSC, (M) PAL	27.00	24.54
(B, D, G, H, I, N, N_C) PAL	27.00	29.50

The CLK2 should be derived from a stable clock source, such as a crystal. CLK2 must have at least a ±50ppm accuracy and at least a 60/40% duty cycle to ensure proper

operation. Use of a PLL to generate a “Line Locked” CLK2 input based on the input video is not recommend. (See next section below.)

Cycle Slipping and Real-Time Pixel Jitter

The decoder’s digital PLL allows it to maintain lock and provide high quality Y/C separation even on the poorest quality input video signals. However, this architecture does not provide a “Line Lock Clock” output and should not be used as a timing master for direct interface to another video encoder in a system.

Since the decoder uses a fixed CLK2 input frequency, the output pixel rate must be periodically adjusted to compensate for any frequency error between CLK2 and the input video signal. This output pixel rate adjustment is referred to as cycle slipping. Since the decoder has an output data FIFO, all cycle slipping can be deferred until the next horizontal blanking interval. This guarantees a consistent number of pixels during the active video region.

Due to cycle slipping, the output timing and data will exhibit a nominal real-time (line-to-line) pixel jitter of one CLK2 period. Although the sample rate converter maintains a 1/8 pixel vertical sample alignment, the output data must be routed to a frame buffer or video compression chip in order remove the effects of cycle slipping. (The frame buffer or compression chip serves as a time base corrector.)

By directly interfacing the decoder to a video encoder, the output video signal will directly reflect the real-time pixel jitter effects of the decoder output timing. The jitter effects can be visualized on a CRT monitor using a static image containing patterns with sharp vertical edges. The edges will appear more “ragged” when compared to the input video signal. The severity of this visual effect relates directly to the frequency error between CLK2 and the input video signal. It is nearly impossible to completely match CLK2 with the input video signal. Therefore, a direct decoder to encoder interface is not recommended.

The use of an external PLL to generate a “Line Locked” CLK2 input derived from the input video signal is also not recommended, since this will defeat the internal digital PLL and result in pixel decoding errors.

Digital Processing of Video

Once the luma and chroma have been separated the HMP8117 then performs programmable modifications (i.e. contrast, coring, color space conversions, color AGC, etc.) to the decoded video signal.

UV to CbCr Conversion

The baseband U and V signals are scaled and offset to generate a nominal range of 16-240 for both the Cb and Cr data.

Digital Color Gain Control

There are four types of color gain control modes available: no gain control, automatic gain control, fixed gain control, and freeze automatic gain control.

If “no gain control” is selected, the amplitude of the color difference signals (CbCr) is not modified, regardless of variations in the color burst amplitude. Thus, a gain of 1x is always used for Cb and Cr.

If “automatic gain control” is selected, the amplitude of the color difference signals (CbCr) is compensated for variations in the color burst amplitude. The burst amplitude is averaged with the two previous lines having a color burst to limit line-to-line variations. A gain of 0.5x to 4x is used for Cb and Cr.

If “fixed gain control” is selected, the amplitude of the color difference signals (CbCr) is multiplied by a constant, regardless of variations in the color burst amplitude. The constant gain value is specified by the COLOR GAIN register $1C_H$. A gain of 0.5x to 4x is used for Cb and Cr. Limiting the gain to 4x limits the amount of amplified noise.

If “freeze automatic gain control” is selected, the amplitude of the color difference signals (CbCr) is multiplied by a constant. This constant is the value the AGC circuitry generated when the “freeze automatic gain” command was selected.

Color Killer

If “enable color killer” is selected, the color output is turned off when the running average of the color burst amplitude is below approximately 25% of nominal for four consecutive fields. When the running average of the color burst amplitude is above approximately 25% of nominal for four consecutive fields, the color output is turned on. The color output is also turned off when excessive phase error of the chroma PLL is present.

If “force color off” is selected, color information is never present on the outputs.

If “force color on” is selected, color information is present on the outputs regardless of the color burst amplitude or chroma PLL phase error.

Y Processing

The black level is subtracted from the luminance data to remove sync and any blanking pedestal information. Negative values of Y are supported at this point to allow proper decoding of “below black” luminance levels.

Scaling is done to position black at 8-bit code 0 and white at 8-bit code 219.

A chroma trap filter may be used to remove any residual color subcarrier from the luminance data. The center frequency of the chroma trap is automatically determined from the video standard being decoded. The chroma trap should be disabled during S-video operation to maintain maximum luminance bandwidth. Alternately, a 3MHz low-pass filter may be used to

remove high-frequency Y data. This may make a noisy image more pleasing to the user, although softer.

Coring of the high-frequency Y data may be done to reduce low-level high frequency noise.

Coring of the Y data may also be done to reduce low-level noise around black. This forces Y data with the following values to a value of 0:

coring = 1: ± 1
coring = 2: ± 1, ± 2
coring = 3: ± 1, ± 2. ± 3

High-frequency components of the luminance signal may be “peaked” to control the sharpness of the image. Maximum gain may be selected to occur at either 2.6MHz or the color subcarrier frequency. This may be used to make the displayed image more pleasing to the user. It should not be used if the output video will be compressed, as the circuit introduces high-frequency components that will reduce the compression ratio.

The brightness control adds or subtracts a user-specified DC offset to the Y data. The contrast control multiplies the Y data by a user-specified amount. These may be used to make the displayed image more pleasing to the user.

Finally, a value of 16 is added to generate a nominal range of 16 (black) to 235 (white).

CbCr Processing

The CbCr data is low-pass filtered to either 0.85MHz or 1.5MHz.

Coring of the CbCr data may be done to reduce low-level noise around zero. This forces CbCr data with the following values to a value of 128.

coring = 1: 127, 129
coring = 2: 126, 127, 129, 130
coring = 3: 125, 126, 127, 129, 130, 131

The saturation control multiplies the CbCr data by a user-specified amount. This may be used to make the displayed image more pleasing to the user. The CbCr data may also be optionally multiplied by the contrast value to avoid color shifts when changing contrast.

The hue control provides a user-specified phase offset to the color subcarrier during decoding. This may be used to correct slight hue errors due to transmission.

YCbCr Output Format Processing

Y has a nominal range of 16 to 235. Cb and Cr have a nominal range of 16 to 240, with 128 corresponding to zero. Values less than 1 are made 1 and values greater than 254 are made 254.

While $\overline{\text{BLANK}}$ is asserted, Y is forced to have a value of 16, with Cb and Cr forced to have a value of 128, unless VBI data is present.

RGB Output Format Processing

The 4:2:2 YCbCr data is converted to 4:4:4 YCbCr data and then converted to either 15-bit or 16-bit gamma-corrected RGB (R′G′B′) data. While $\overline{\text{BLANK}}$ is asserted, RGB data is forced to a value of 0.

15-Bit R′G′B′

The following YCbCr to R′G′B′ equations are used to maintain the proper black and white levels:

R′ = 0.142(Y - 16) + 0.194(Cr - 128)
G′ = 0.142(Y - 16) - 0.099(Cr - 128) - 0.048(Cb - 128)
B′ = 0.142(Y - 16) + 0.245(Cb - 128)

The resulting 15-bit R′G′B′ data has a range of 0 to 31. Values less than 0 are made 0 and values greater than 31 are made 31.

The 15-bit R′G′B′ data may be converted to 15-bit linear RGB, using the following equations. Although the PAL specifications specify a gamma of 2.8, a gamma of 2.2 is normally used. The HMP8117 allows the selection of the gamma to be either 2.2 or 2.8, independent of the video standard.

for gamma = 2.2:

for R′G′B′ < 0.0812*31
R = (31)((R′/31)/4.5)
G = (31)((G′/31)/4.5)
B = (31)((B′/31)/4.5)

for R′G′B′ >= 0.0812*31
$R = (31)(((R'/31) + 0.099)/1.099)^{2.2}$
$G = (31)(((G'/31) + 0.099)/1.099)^{2.2}$
$B = (31)(((B'/31) + 0.099)/1.099)^{2.2}$

for gamma = 2.8:

$R = (31)(R'/31)^{2.8}$
$G = (31)(G'/31)^{2.8}$
$B = (31)(B'/31)^{2.8}$

16-Bit R′G′B′

The following YCbCr to R′G′B′ equations are used to maintain the proper black and white levels:

R′ = 0.142(Y - 16) + 0.194(Cr - 128)
G′ = 0.288(Y - 16) - 0.201(Cr - 128) - 0.097(Cb - 128)
B′ = 0.142(Y - 16) + 0.245(Cb - 128)

The resulting 16-bit R′G′B′ data has a range of 0 to 31 for R′ and B′, and a range of 0 to 63 for G′. Values less than 0 are made 0; R′ and B′ values greater than 31 are made 31, G′ values greater than 63 are made 63.

The 16-bit R′G′B′ data may be converted to 16-bit linear RGB, using the following equations. Although the PAL specifications specify a gamma of 2.8, a gamma of 2.2 is normally used. The HMP8117 allows the selection of the gamma to be either 2.2 or 2.8, independent of the video standard.

for gamma = 2.2:

for R′B′ < 0.0812*31, G′ < 0.0812*63

R = (31)((R′/31)/4.5)

G = (63)((G′/63)/4.5)

B = (31)((B′/31)/4.5)

for R′B′ >= 0.0812*31, G′ >= 0.0812*63

$R = (31)(((R'/31) + 0.099)/1.099)^{2.2}$

$G = (63)(((G'/63) + 0.099)/1.099)^{2.2}$

$B = (31)(((B'/31) + 0.099)/1.099)^{2.2}$

for gamma = 2.8:

$R = (31)(R'/31)^{2.8}$

$G = (63)(G'/63)^{2.8}$

$B = (31)(B'/31)^{2.8}$

Built-in Video Generation

The decoder can be configured to output a full-screen of built-in blue, black or 75% color bar patterns. The type of pattern generated is determined by bits 2-1 of the OUTPUT FORMAT register 02_H. When built-in video generation is not desired, the bits need to be set for normal operation to pass decoded video.

If the decoder is currently locked to a video source on the input, the output data timing will be based on the input video source. If an input video source is not detected, internally-generated output data timing will be used. The following table lists the data codes output for each built-in video pattern in YCbCr format.

TABLE 2. BUILT-IN VIDEO PATTERN DATA CODES

PATTERN: COLOR	Y	Cb	Cr
75% Color Bar: White	$B4_H$	80_H	80_H
Yellow	$A2_H$	$2C_H$	$8E_H$
Cyan	83_H	$9C_H$	$2C_H$
Green	70_H	48_H	$3A_H$
Magenta	54_H	$B8_H$	$C6_H$
Red	41_H	64_H	$D4_H$
Blue	23_H	$D4_H$	72_H
Black	10_H	80_H	80_H
Blue Screen: Blue	$4B_H$	$D9_H$	88_H
Black Screen: Black	10_H	80_H	80_H

Pixel Port Timing

The the timing and format of the output data and control signals is presented in the following sections. Refer to the section “CYCLE SLIPPING AND REAL-TIME PIXEL JITTER” for PLL and interface considerations.

$\overline{HSYNC}$ and $\overline{VSYNC}$ Timing

The $\overline{HSYNC}$ and $\overline{VSYNC}$ output timing is VMI v1.4 compatible. Figures 3-6 illustrate the video timing. The leading edge of $\overline{HSYNC}$ is synchronous to the video input signal and has a fixed latency due to internal pipeline processing. The pulse width of the $\overline{HSYNC}$ is defined by the END HSYNC register 36_H, where the trailing edge of $\overline{HSYNC}$ has a programmable delay of 0-510 CLK2 cycles from the leading edge.

The leading edge of $\overline{VSYNC}$ is asserted approximately half way through the first serration pulse of each field. An accumulator is used to detect a low-time period within the serration pulse. Since the leading edge of $\overline{VSYNC}$ is detected, it should not be used for timing with respect to $\overline{HSYNC}$ or $\overline{BLANK}$.

The trailing edge of $\overline{VSYNC}$ implements the VMI handshake with $\overline{HSYNC}$ in order to determine field information without using the FIELD pin. For an odd field, the trailing edge of $\overline{VSYNC}$ is 5 ±1 CLK2 cycles after the trailing edge of the $\overline{HSYNC}$ that follows the last equalization pulse. Refer to Figures 3 and 5. For an even field, the trailing edge of $\overline{VSYNC}$ is 5 ±1 CLK2 cycles after the leading edge of the $\overline{HSYNC}$ that follows the last equalization pulse. Refer to Figures 4 and 6.

Field Timing

When field information can be determined from the input video source, the FIELD output pin reflects the video source field state. When field information cannot be determined from the input video source, the FIELD output pin alternates its state at the beginning of each field. FIELD changes state 5±1 CLK2 cycles before the leading edge of $\overline{VSYNC}$.

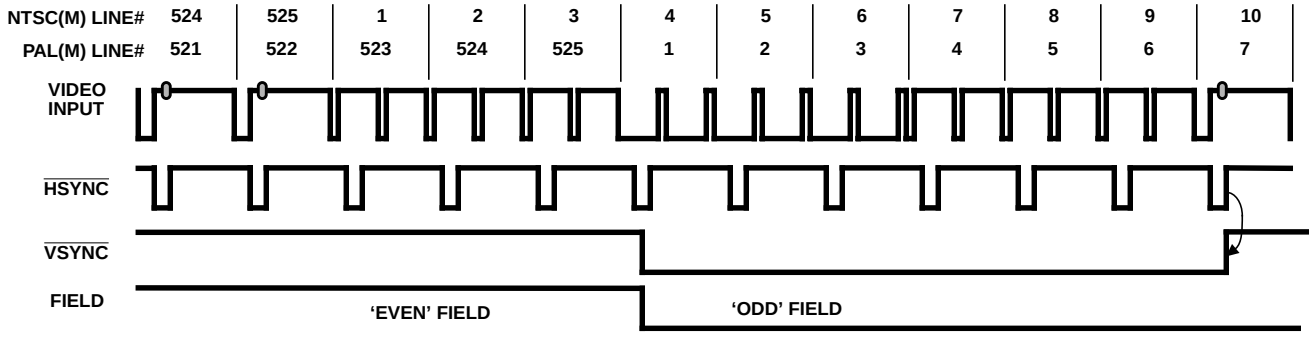


FIGURE 3. NTSC(M) AND PAL(M) ODD FIELD TIMING

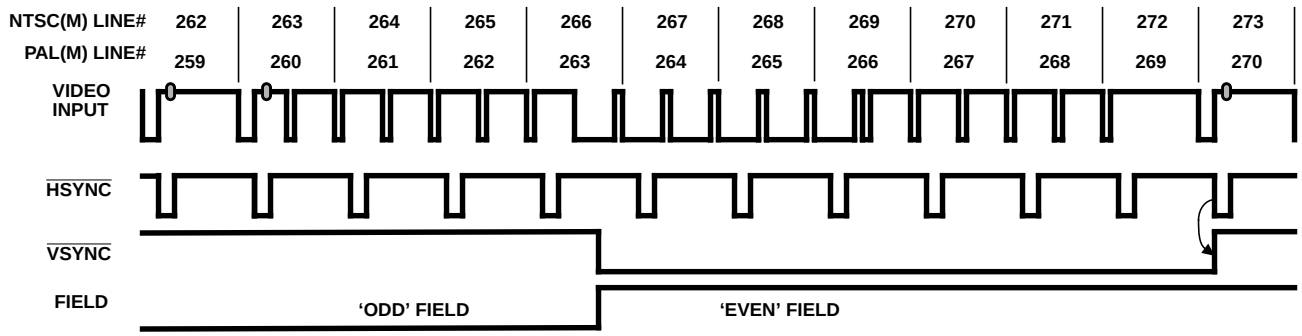


FIGURE 4. NTSC(M) AND PAL(M) EVEN FIELD TIMING

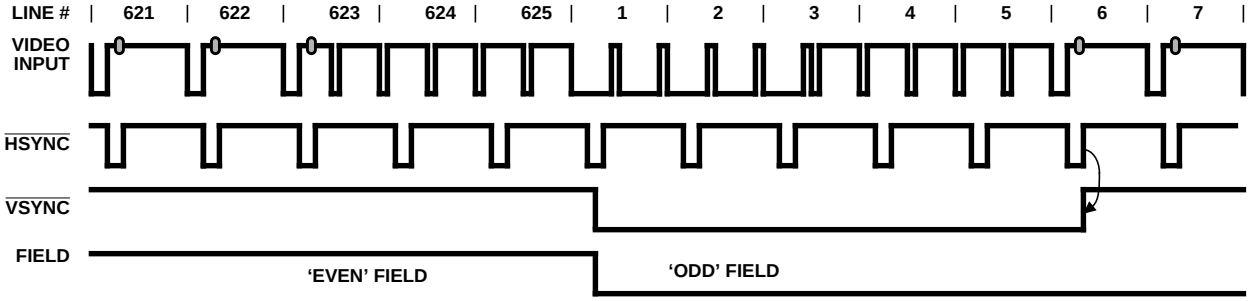


FIGURE 5. PAL(B, D, G, H, I, N, N_C) ODD FIELD TIMING

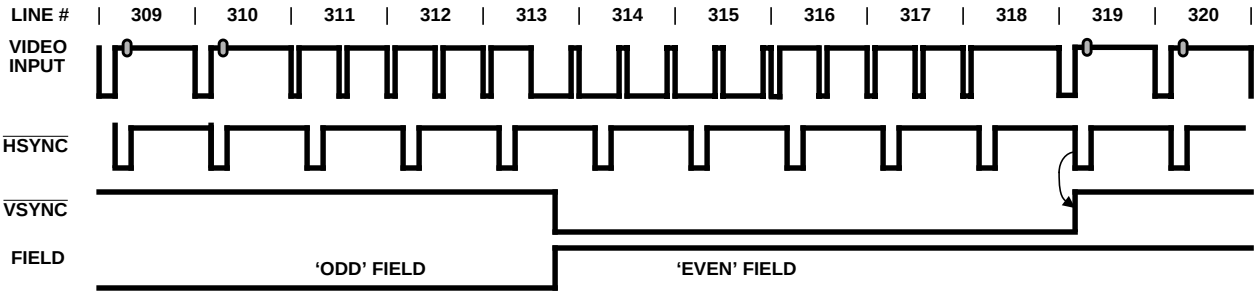


FIGURE 6. PAL(B, D, G, H, I, N, N_C) EVEN FIELD TIMING

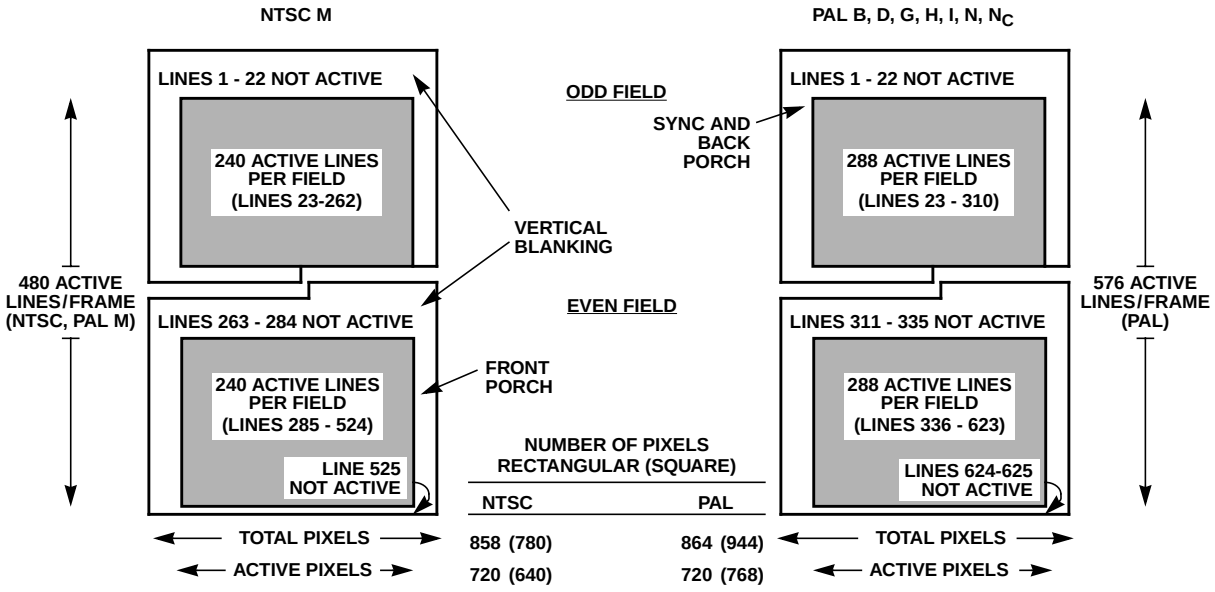
$\overline{BLANK}$ and $\overline{DVALID}$ Timing

$\overline{DVALID}$ is asserted when P15-P0 contain valid data. The behavior of the $\overline{DVALID}$ output is determined by bit 4 (DVLD_LTC) and bit 5 (DLVD_DCYC) of the GENLOCK CONTROL register 04_H for each video output mode.

The $\overline{BLANK}$ output pin is used to distinguish the blanking interval period from active video data. The blanking intervals are programmable in both horizontal and vertical dimensions. Reference Figure 7 for active video timing and use Table 3 for typical blanking programming values.

During active scan lines, $\overline{BLANK}$ is asserted when the horizontal pixel count matches the value in the START H_BLANK register $31_H/30_H$. The pixel counter is 000_H at the leading edge of the sync tip after a fixed pipeline delay. Since blanking normally occurs on the front porch, (prior to count 000H) the START H_BLANK count must be programmed with a large value from the previous line. Refer to the Last Pixel Count from Table 3. $\overline{BLANK}$ is negated when the horizontal pixel count matches the value in the END H_BLANK register 32_H. Note that horizontally, $\overline{BLANK}$ is programmable with two pixel resolution.

START V_BLANK register $34_H/33_H$ and END V_BLANK register 35_H determine which scan lines are blanked for each field. During inactive scan lines, $\overline{BLANK}$ is asserted during the entire scan line. Half-line blanking of the output video cannot be done.



NOTE:

3. The line numbering for PAL (M) is the NTSC (M) line count minus 3 per the video standards.

FIGURE 7. TYPICAL ACTIVE VIDEO REGIONS

TABLE 3. TYPICAL VALUES FOR H_BLANK AND V_BLANK REGISTERS

VIDEO STANDARD (MSB/LSB)	ACTIVE PIXELS/ LINE	TOTAL PIXELS/ LINE	LAST PIXEL COUNT	START H_BLANK (31H/30H)	END H_BLANK (32H)	START V_BLANK (34H/33H)	END V_BLANK (35H)
RECTANGULAR PIXELS							
NTSC (M), PAL (M)	720	858	857 (0359_H)	842 ($034A_H$)	122 ($7A_H$)	259 (0103_H)	19 (13_H)
PAL (B, D, G, H, I, N, N_C)	720	864	863 ($035F_H$)	852 (0354_H)	132 (84_H)	310 (0136_H)	22 (16_H)
SQUARE PIXELS							
NTSC (M), PAL (M)	640	780	779 ($030B_H$)	758 ($02F6_H$)	118 (76_H)	259 (0103_H)	19 (13_H)
PAL (B, D, G, H, I, N, N_C)	768	944	943 ($03AF_H$)	922 ($039A_H$)	154 ($9A_H$)	310 (0136_H)	22 (16_H)

TABLE 4. PIXEL OUTPUT FORMATS

PIN NAME	8-BIT, 4:2:2, YCbCr	16-BIT, 4:2:2, YCbCr	15-BIT, RGB, (5,5,5)	16-BIT, RGB, (5,6,5)	BT.656
P0	0 [0]	Cb0, Cr0 [$D0_{n+1}$]	B0 [$D0_{n+1}$]	B0 [$D0_{n+1}$]	0 [0]
P1	0 [0]	Cb1, Cr1 [$D1_{n+1}$]	B1 [$D1_{n+1}$]	B1 [$D1_{n+1}$]	0 [0]
P2	0 [0]	Cb2, Cr2 [$D2_{n+1}$]	B2 [$D2_{n+1}$]	B2 [$D2_{n+1}$]	0 [0]
P3	0 [0]	Cb3, Cr3 [$D3_{n+1}$]	B3 [$D3_{n+1}$]	B3 [$D3_{n+1}$]	0 [0]
P4	0 [0]	Cb4, Cr4 [$D4_{n+1}$]	B4 [$D4_{n+1}$]	B4 [$D4_{n+1}$]	0 [0]
P5	0 [0]	Cb5, Cr5 [$D5_{n+1}$]	G0 [$D5_{n+1}$]	G0 [$D5_{n+1}$]	0 [0]
P6	0 [0]	Cb6, Cr6 [$D6_{n+1}$]	G1 [$D6_{n+1}$]	G1 [$D6_{n+1}$]	0 [0]
P7	0 [0]	Cb7, Cr7 [$D7_{n+1}$]	G2 [$D7_{n+1}$]	G2 [$D7_{n+1}$]	0 [0]
P8	Y0, Cb0, Cr0 [D0]	Y0 [$D0_n$]	G3 [$D0_n$]	G3 [$D0_n$]	YCbCr Data, Ancillary Data, SAV and EAV Sequences [D0 - D7, where P8 corresponds to D0]
P9	Y1, Cb1, Cr1 [D1]	Y1 [$D1_n$]	G4 [$D1_n$]	G4 [$D1_n$]	
P10	Y2, Cb2, Cr2 [D2]	Y2 [$D2_n$]	R0 [$D2_n$]	G5 [$D2_n$]	
P11	Y3, Cb3, Cr3 [D3]	Y3 [$D3_n$]	R1 [$D3_n$]	R0 [$D3_n$]	
P12	Y4, Cb4, Cr4 [D4]	Y4 [$D4_n$]	R2 [$D4_n$]	R1 [$D4_n$]	
P13	Y5, Cb5, Cr5 [D5]	Y5 [$D5_n$]	R3 [$D5_n$]	R2 [$D5_n$]	
P14	Y6, Cb6, Cr6 [D6]	Y6 [$D6_n$]	R4 [$D6_n$]	R3 [$D6_n$]	
P15	Y7, Cb7, Cr7 [D7]	Y7 [$D7_n$]	0 [$D7_n$]	R4 [$D7_n$]	

NOTE:

4. Definitions in brackets are port definitions during raw VBI data transfers. Refer to the section on teletext for more information on raw VBI.

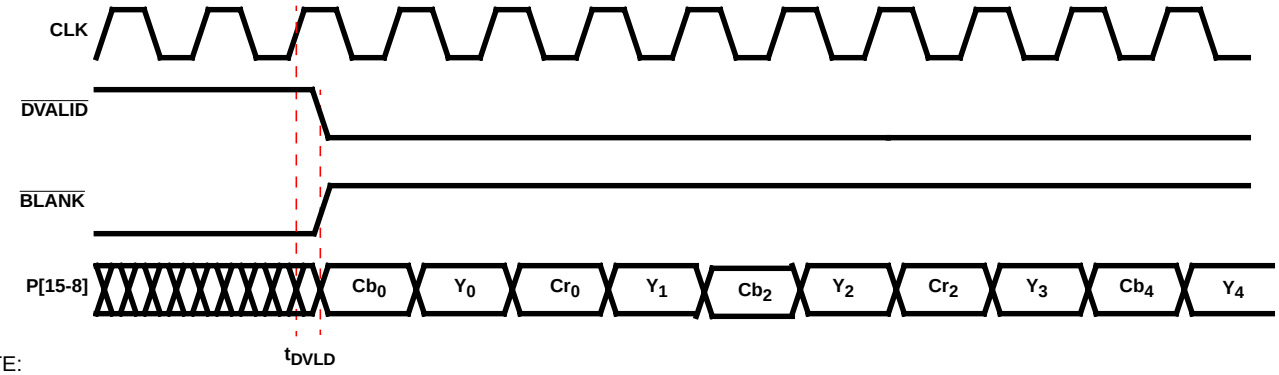
Pixel Output Port

Pixel data is output via the P0-P15 pins. Refer to Table 4 for the output pin definition as a function of the output mode. Refer to the section “CYCLE SLIPPING AND REAL-TIME PIXEL JITTER” for PLL and interface considerations.

8-Bit YCbCr Output

Each YCbCr data byte is output following each rising edge of CLK2. The YCbCr data is multiplexed as [Cb Y Cr Y′ Cb Y Cr Y′...], with the first active data each scan line containing Cb data. The pixel output timing is shown in Figures 8 and 9.

$\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{DVALID}}$, $\overline{\text{VBIVALID}}$, and FIELD are output following the rising edge of CLK2. When $\overline{\text{BLANK}}$ is asserted and $\overline{\text{VBIVALID}}$ is deasserted, the YCbCr outputs have a value of 16 for Y and 128 for Cb and Cr. The behavior of the $\overline{\text{DVALID}}$ output is determined by bit 4 (DVLD_LTC) of the GENLOCK CONTROL register 04_H.



NOTE:

5. Y_0 is the first active luminance pixel data of a line. Cb_0 and Cr_0 are first active chrominance pixel data in a line. Cb and Cr will alternate every cycle due to the 4:2:2 subsampling. Pixel data is not output during the blanking period, but the values are forced to blanking levels.

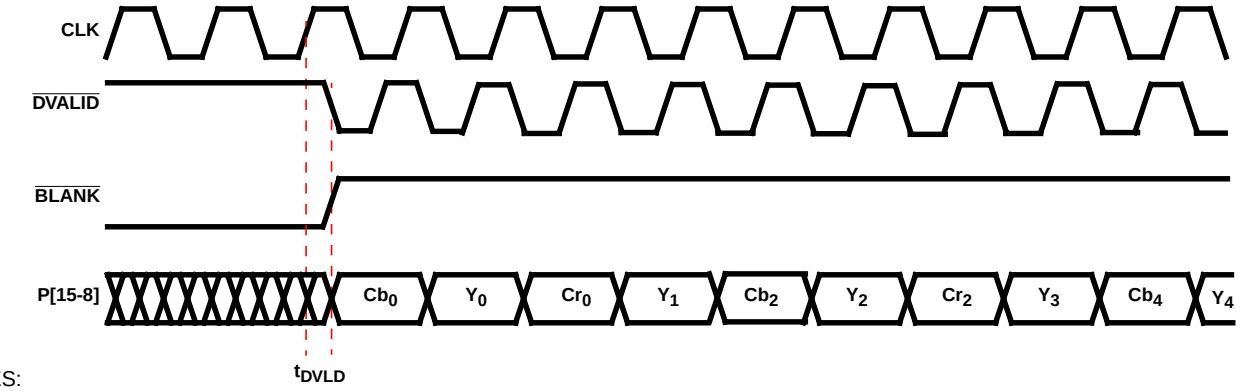
FIGURE 8. OUTPUT TIMING FOR 8-BIT YCbCr MODE (DVLD_LTC = 0)

16-Bit YCbCr, 15-Bit RGB, or 16-RGB Output

For 16-bit YCbCr, 15-bit RGB data, or 16-bit RGB output modes, the data is output following the rising edge of CLK2 with $\overline{\text{DVALID}}$ asserted. Either linear or gamma-corrected RGB data may be output. The pixel output timing is shown in Figures 10 to 13.

$\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{DVALID}}$, $\overline{\text{VBIVALID}}$, and FIELD are output following the rising edge of CLK2. When $\overline{\text{BLANK}}$ is asserted and $\overline{\text{VBIVALID}}$ is deasserted, the YCbCr outputs have a value of 16 for Y and 128 for Cb and Cr; the RGB outputs have a value of 0.

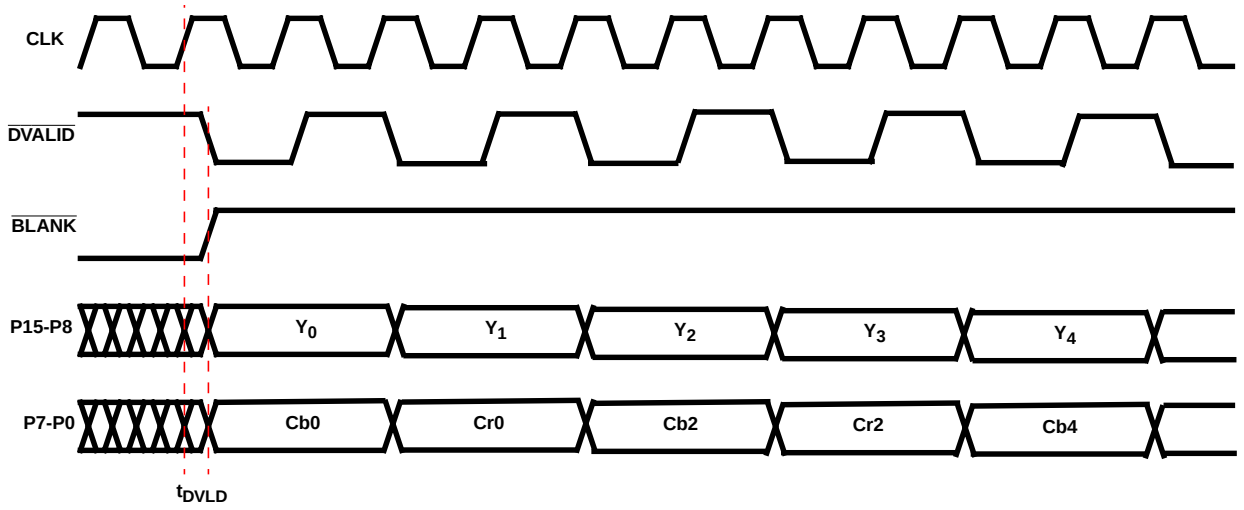
The behavior of the $\overline{\text{DVALID}}$ output is determined by bit 4 (DVLD_LTC) and bit 5 (DLVD_DCYC) of the GENLOCK CONTROL register 04_H.



NOTES:

6. Y_0 is the first active luminance pixel data of a line. Cb_0 and Cr_0 are first active chrominance pixel data in a line. Cb and Cr will alternate every cycle due to the 4:2:2 subsampling. Pixel data is not output during the blanking period, but the values are forced to blanking levels.
7. When DVLD_LTC is set to 1, the polarity of $\overline{\text{DVALID}}$ needs to be set to active low, otherwise $\overline{\text{DVALID}}$ will stay low during active video and be gated with the clock only during the blanking interval.

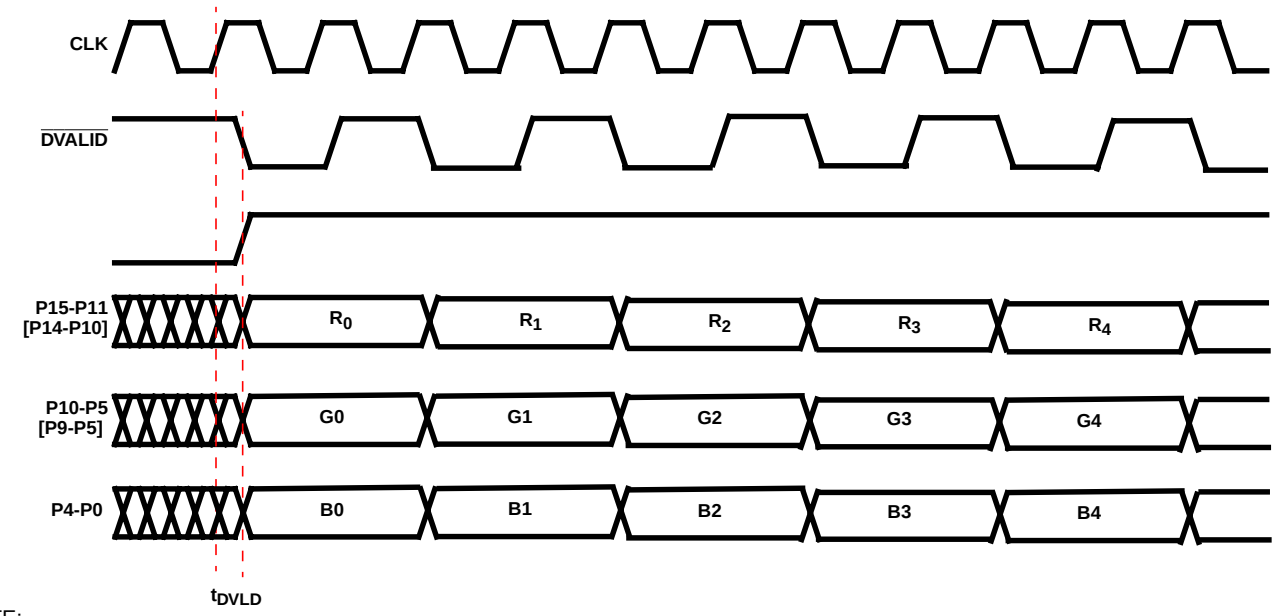
FIGURE 9. OUTPUT TIMING FOR 8-BIT YCbCr MODE (DVLD_LTC = 1)



NOTES:

8. Y_0 is the first active luminance pixel data of a line. Cb_0 and Cr_0 are first active chrominance pixel data in a line. Cb and Cr will alternate every cycle due to the 4:2:2 subsampling.
9. $\overline{BLANK}$ is asserted per Figure 7.

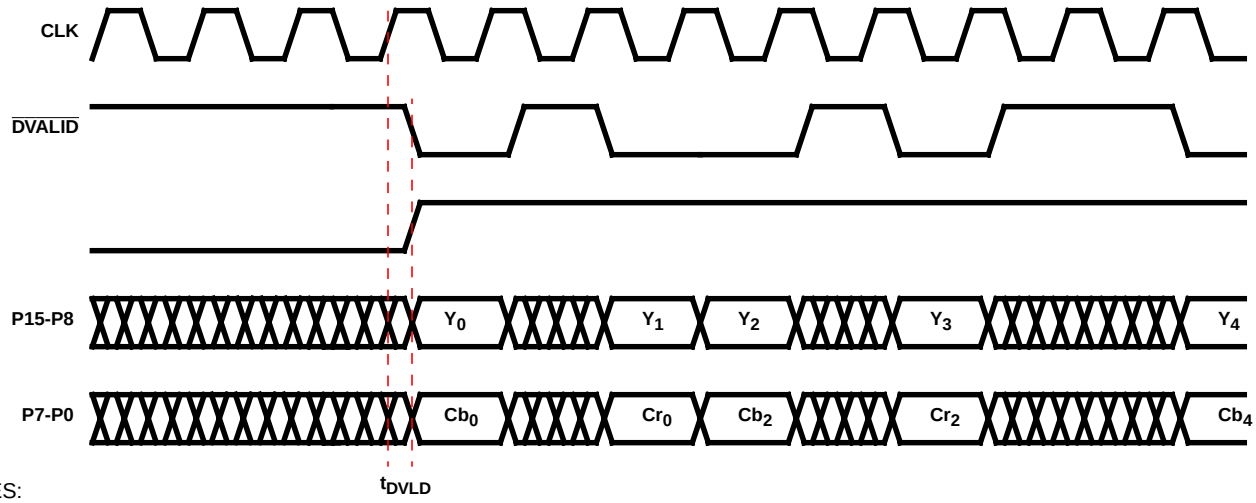
FIGURE 10. OUTPUT TIMING FOR 16-BIT YCbCr MODE (DVLD_LTC = 0, DVLD_DCYC = 0)



NOTE:

10. $\overline{BLANK}$ is asserted per Figure 7.

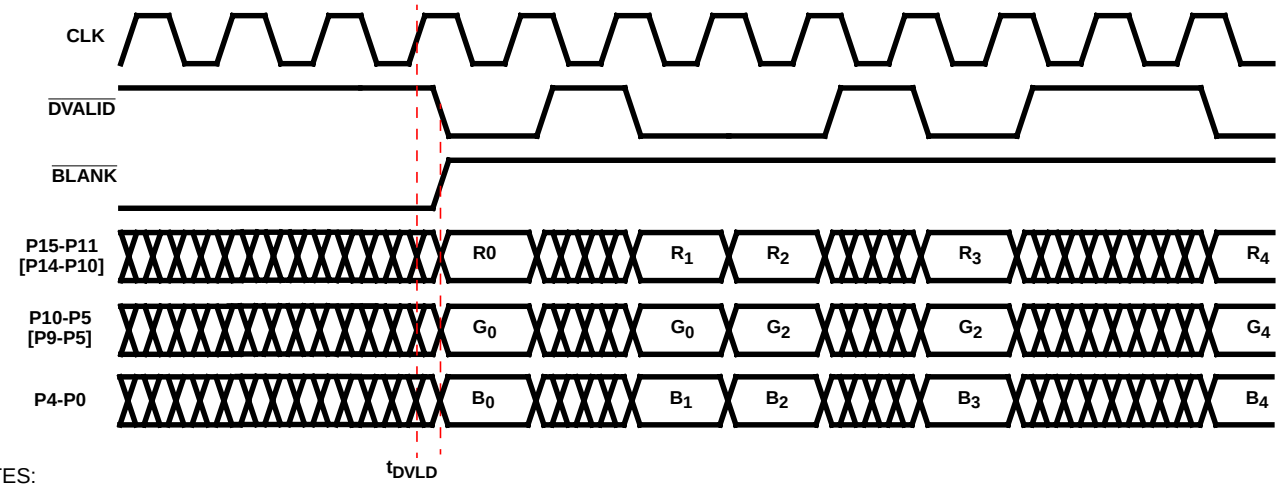
FIGURE 11. OUTPUT TIMING FOR 16-BIT [15-BIT] RGB MODE (DVLD_LTC = 0, DVLD_DCYC = 0)



NOTES:

11. Y_0 is the first active luminance pixel of a line. Cb_0 and Cr_0 are first active chrominance pixels in a line. Cb and Cr will alternate every cycle due to the 4:2:2 subsampling.
12. $\overline{BLANK}$ is asserted per Figure 7.
13. $\overline{DVALID}$ is asserted for every valid pixel during both active and blanking regions.

FIGURE 12. OUTPUT TIMING FOR 16-BIT YCbCr MODE (DVLD_LTC = 0, DVLD_DCYC = 1)



NOTES:

14. $\overline{BLANK}$ is asserted per Figure 7.
15. $\overline{DAVLID}$ is asserted for every valid pixel during both active and blanking regions. $\overline{DVALID}$ is not a 50% duty cycle synchronous output and will appear to jitter as the Output Sample Rate converter adjusts the output timing for various data rates and clock frequency inputs.

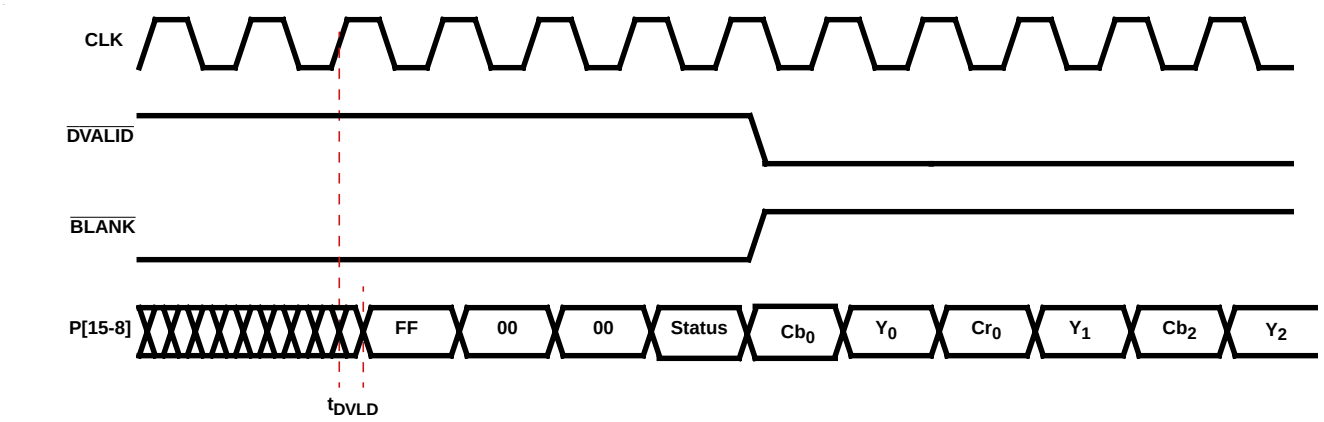
FIGURE 13. OUTPUT TIMING FOR 16-BIT [15-BIT] RGB MODE (DVLD_LTC = 0, DVLD_DCYC = 1)

8-Bit BT.656 Output

For the BT.656 output mode, data is output following each rising edge of CLK2. The BT.656 EAV and SAV formats are shown in Table 5 and the pixel output timing is shown in Figure 14. The EAV and SAV timing is determined by the programmed horizontal and vertical blank timing.

$\overline{BLANK}$, $\overline{HSYNC}$, $\overline{VSYNC}$, $\overline{DVALID}$, $\overline{VBIVALID}$, and FIELD are output following the rising edge of CLK2.

During the blanking intervals, the YCbCr outputs have a value of 16 for Y and 128 for Cb and Cr, unless ancillary data is present.



NOTES:

16. Y_0 is the first active luminance pixel data of a line. Cb_0 and Cr_0 are first active chrominance pixel data in a line. Cb and Cr will alternate every cycle due to the 4:2:2 subsampling. Pixel data is not output during the blanking period.
17. Notice that $\overline{\text{DVALID}}$ is not asserted during the preamble and that $\overline{\text{BLANK}}$ is still asserted.
18. See table 5 for Status bit definitions.

FIGURE 14. OUTPUT TIMING FOR 8-BIT BT.656 MODE

TABLE 5. BT.656 EAV AND SAV SEQUENCES

PIXEL INPUT	P15	P14	P13	P12	P11	P10	P9	P8
Preamble	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0
Status Word	1	F	V	H	P3	P2	P1	P0

NOTES:

19. P3 = V xor H; P2 = F xor H; P1 = F xor V; P0 = F xor V xor H
20. F: “0” = field 1; “1” = field 2
21. V: “1” during vertical blanking
22. H: “0” at SAV (start of active video); “1” at EAV (end of active video)

Advanced Features

In addition to digitizing an analog video signal the HMP8117 has hardware to process different types of Vertical Blanking Interval (VBI) data as described in the following sections.

“Sliced” VBI Data Capture

The HMP8117 implements “sliced” data capture of select types of VBI data. The VBI decoders incorporate detection hysteresis to prevent them from rapidly turning on and off due to noise and transmission errors. In order to handle real-world signals, the VBI decoders also compensate for DC offsets and amplitude variations.

Closed Captioning

During closed captioning capture, the scan lines containing captioning information are monitored. If closed captioning is enabled and captioning data is present, the caption data is loaded into the caption data registers.

DETECTION OF CLOSED CAPTIONING

The closed caption decoder monitors the appropriate scan lines looking for the clock run-in and start bits used by captioning. If found, it locks to the clock run-in, the caption data is sampled and loaded into shift registers, and the data is then transferred to the caption data registers.

If the clock run-in and start bits are not found, it is assumed the scan line contains video data unless other VBI information is detected, such as teletext.

Once the clock run-in and start bits are found on the appropriate scan line for four consecutive odd fields, the Closed Captioning odd field Detect status bit is set to “1”. It is reset to “0” when the clock run-in and start bits are not found on the appropriate scan lines for four consecutive odd fields.

Once the clock run-in and start bits are found on the appropriate scan line for four consecutive even fields, the Closed Captioning even field Detect status bit is set to “1”. It is reset to “0” when the clock run-in and start bits are not found on the appropriate scan lines for four consecutive even fields.

READING THE CAPTION DATA

The caption data registers may be accessed in two ways: via the I^2C interface or as BT.656 ancillary data.

CAPTIONING DISABLED ON BOTH LINES

In this case, any caption data present is ignored.

The Caption odd field Read status bit and the Caption even field Read status bit are always a “0”.

ODD FIELD CAPTIONING

In this case, any caption data present on line 284 (or line 281 or 335 in the PAL modes) is ignored. Caption data present on line 21 (or line 18 or 22 in the PAL modes) is captured into a shift register then transferred to CLOSED CAPTION_ODD_A register 20_H and CLOSED CAPTION_ODD_B register 21_H.

The Caption even field Read status bit is always a “0”. The Caption odd field Read status bit is set to “1” after data has been transferred from the shift register to the CLOSED CAPTION_ODD_A and CLOSED CAPTION_ODD_B registers. It is set to “0” after the data has been read out.

EVEN FIELD CAPTIONING

In this case, any caption data present on line 21 (or line 18 or 22 in the PAL modes) is ignored. Caption data present on line 284 (or line 281 or 335 in the PAL modes) is captured into a shift register then transferred to CLOSED CAPTION_EVEN_A register 22_H and CLOSED CAPTION_EVEN_B register 23_H.

The Caption odd field Read status bit is always a “0”. The Caption even field Read status bit is set to “1” after data has been transferred from the shift register to the CLOSED CAPTION_EVEN_A and CLOSED CAPTION_EVEN_B registers. It is set to “0” after the data has been read out.

ODD AND EVEN FIELD CAPTIONING

Caption data present on line 21 (or line 18 or 22 in the PAL modes) is captured into a shift register then transferred to the CLOSED CAPTION_ODD_A and CLOSED CAPTION_ODD_B registers. Caption data present on line 284 (or line 281 or 335 in the PAL modes) is captured into a shift register then transferred to the CLOSED CAPTION_EVEN_A and CLOSED CAPTION_EVEN_B registers.

The Caption odd field Read status bit is set to “1” after data has been transferred from the shift register to the CLOSED CAPTION_ODD_A and CLOSED CAPTION_ODD_B registers. It is set to “0” after the data has been read out.

The Caption even field Read status bit is set to “1” after data has been transferred from the shift register to the CLOSED CAPTION_EVEN_A and CLOSED CAPTION_EVEN_B registers. It is set to “0” after the data has been read out.

Widescreen Signalling (WSS)

During WSS capture (ITU-R BT.1119 and EIAJ CPX-1204), the scan lines containing WSS information are monitored. If WSS is enabled and WSS data is present, the WSS data is loaded into the WSS data registers.

DETECTION OF WSS

The WSS decoder monitors the appropriate scan lines looking for the run-in and start codes used by WSS. If found, it locks to the run-in code, the WSS data is sampled and loaded into shift registers, and the data is then transferred to the WSS data registers.

If the run-in and start codes are not found, it is assumed the scan line contains video data unless other VBI information is detected, such as teletext.

Once the run-in and start codes are found on the appropriate scan line for four consecutive odd fields, the WSS Line 20 Detect status bit is set to “1”. It is reset to “0” when the run-in and start codes are not found on the appropriate scan lines for four consecutive odd fields.

Once the run-in and start codes are found on the appropriate scan line for four consecutive even fields, the WSS Line 283 Detect status bit is set to “1”. It is reset to “0” when the clock run-in and start bits are not found on the appropriate scan lines for four consecutive even fields.

READING THE WSS DATA

The WSS data registers may be accessed in two ways: via the I^2C interface or as BT.656 ancillary data.

WSS DISABLED ON BOTH LINES

In this case, any WSS data present is ignored.

The WSS odd field Read status bit and the WSS even field Read status bit are always a “0”.

ODD FIELD WSS

In this case, any WSS data present on line 283 (or line 280 or 336 in the PAL modes) is ignored. WSS data present on line 20 (or line 17 or 23 in the PAL modes) is captured into a shift register then transferred to the WSS_ODD_A and WSS_ODD_B data registers.

The WSS even field Read status bit is always a “0”. The WSS odd field Read status bit is set to “1” after data has been transferred from the shift register to the WSS_ODD_A and WSS_ODD_B registers. It is set to “0” after the data has been read out.

EVEN FIELD WSS

In this case, any WSS data present on line 20 (or line 17 or 23 in the PAL modes) is ignored. WSS data present on line 283 (or line 280 or 336 in the PAL modes) is captured into a shift register then transferred to the WSS_EVEN_A and WSS_EVEN_B data registers.

The WSS odd field Read status bit is always a “0”. The WSS even field Read status bit is set to “1” after data has been transferred from the shift register to the WSS_EVEN_A and WSS_EVEN_B registers. It is set to “0” after the data has been read out.

ODD AND EVEN WSS

WSS data present on line 20 (or line 17 or 23 in the PAL modes) is captured into a shift register then transferred to the WSS_ODD_A and WSS_ODD_B registers. WSS data present on line 283 (or line 280 or 336 in the PAL modes) is captured into a shift register then transferred to the WSS_EVEN_A and WSS_EVEN_B registers.

The WSS odd field Read status bit is set to “1” after data has been transferred from the shift register to the WSS_ODD_A and WSS_ODD_B registers. It is set to “0” after the data has been read out.

The WSS even field Read status bit is set to “1” after data has been transferred from the shift register to the WSS_EVEN_A and WSS_EVEN_B registers. It is set to “0” after the data has been read out.

BT.656 Ancillary Data

Through the BT.656 interface the HMP8117 can generate non-active video data which contains CC, WSS, teletext or Real-Time Control Interface (RTCI) information. Teletext and RTCI data is only available as BT.656 ancillary data.

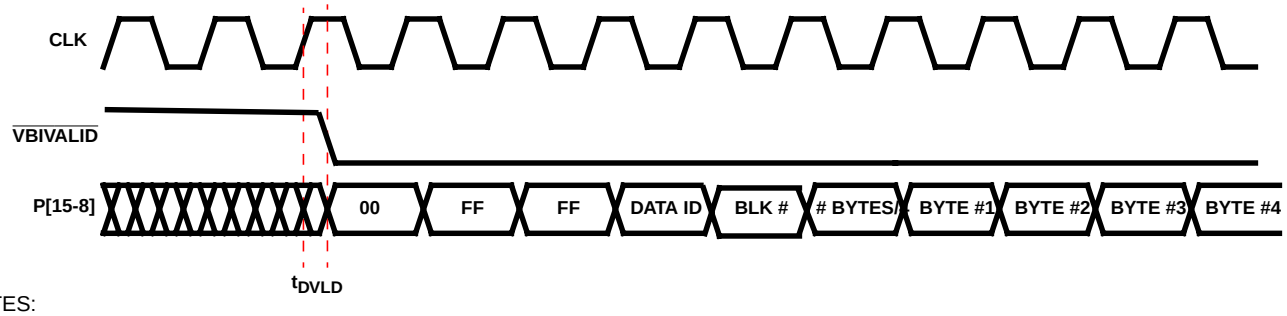
$\overline{\text{VBIVALID}}$ Output Timing

The $\overline{\text{VBIVALID}}$ output is asserted when outputting Closed Captioning, Wide Screen Signalling, Teletext or RTCI data as BT.656 ancillary data. It is asserted during the entire BT.656 ancillary data packet time, including the preamble.

BT.656 Closed Captioning and Wide Screen Signalling

Table 6 illustrates the format when outputting the caption data registers as BT.656 ancillary data. The ancillary data is present during the horizontal blanking interval after the line containing the captioning information.

Table 7 illustrates the format when outputting the WSS data registers as BT.656 ancillary data. The ancillary data is present during the horizontal blanking interval after the line containing the WSS information.



NOTES:

23. BT.656 VBI ancillary starts with a 00H, FFH and FFH sequence which is opposite to the SAV/EAV sequence of FFH, 00H and 00H.

24. During active VBI data intervals, $\overline{\text{DVALID}}$ is deasserted and $\overline{\text{BLANK}}$ is asserted.

FIGURE 15. OUTPUT TIMING FOR BT.656 VBI DATA TRANSFERS (CC, WSS, TELETEXT, RTCI)

TABLE 6. READING THE CLOSED CAPTION DATA AS BT.656 ANCILLARY DATA

PIXEL OUTPUT	P15	P14	P13	P12	P11	P10	P9	P8
Preamble	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	1	1
	1	1	1	1	1	1	1	1
Data ID	$\overline{P14}$	ep	1	1	0	0	0	0 = odd field data 1 = even field data
Data Block Number	$\overline{P14}$	ep	0	0	0	0	0	1
Data Word Count	$\overline{P14}$	ep	0	0	0	0	0	1
Caption Data	$\overline{P14}$	ep	0	0	bit 15	bit 14	bit 13	bit 12
	$\overline{P14}$	ep	0	0	bit 11	bit 10	bit 9	bit 8
	$\overline{P14}$	ep	0	0	bit 7	bit 6	bit 5	bit 4
	$\overline{P14}$	ep	0	0	bit 3	bit 2	bit 1	bit 0
CRC	$\overline{P14}$	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

NOTES:

25. ep = even parity for P8-P13.

26. CRC = Sum of P8-P14 of Data ID through last user data word. Preset to all zeros, carry is ignored.

TABLE 7. OUTPUTTING THE SLICED WSS DATA AS BT.656 ANCILLARY DATA

PIXEL OUTPUT	P15	P14	P13	P12	P11	P10	P9	P8
Preamble	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	1	1
	1	1	1	1	1	1	1	1
Data ID	$\overline{P14}$	ep	1	1	0	0	1	0 = odd field data 1 = even field data
Data Block Number	$\overline{P14}$	ep	0	0	0	0	0	1
Data Word Count	$\overline{P14}$	ep	0	0	0	0	1	0
WSS Data	$\overline{P14}$	ep	0	0	0	0	bit 13	bit 12
	$\overline{P14}$	ep	0	0	bit 11	bit 10	bit 9	bit 8
	$\overline{P14}$	ep	0	0	bit 7	bit 6	bit 5	bit 4
	$\overline{P14}$	ep	0	0	bit 3	bit 2	bit 1	bit 0
WSS CRC Data	$\overline{P14}$	ep	0	0	0	0	bit 5	bit 4
	$\overline{P14}$	ep	0	0	bit 3	bit 2	bit 1	bit 0
	$\overline{P14}$	ep	0	0	0	0	0	0
	$\overline{P14}$	ep	0	0	0	0	0	0
CRC	$\overline{P14}$	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

NOTES:

27. ep = even parity for P8-P13.

28. WSS CRC data = “00 0000” during PAL operation.

29. CRC = Sum of P8-P14 of Data ID through last user data word. Preset to all zeros, carry is ignored.

Teletext

The HMP8117 supports ITU-R BT.653 625-line and 525-line teletext system B, C and D capture. NABTS (North American Broadcast Teletext Specification) is the same as BT.653 525-line system C, which is also used to transmit Intel Intercast™ information. WST (World System Teletext) is the same as BT.653 system B. Figure 16 shows the basic structure of a video signal that contains teletext data.

The scan lines containing teletext information are monitored. If teletext is enabled and teletext data is present, the teletext data is output as BT.656 ancillary data.

DETECTION OF TELETEXT

The teletext decoder monitors the scan lines, looking for the 16-bit clock run-in (sometimes referred to as the clock synchronization code) used by teletext. If found, it locks to the clock run-in, the teletext data is sampled and loaded into shift registers, and the data is then transferred to internal holding registers.

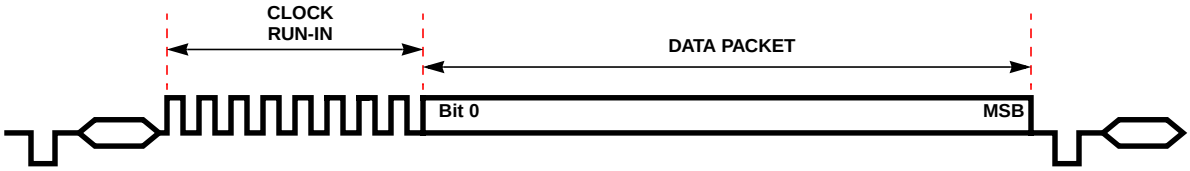
If the clock run-in is not found, it is assumed the scan line contains video data unless other VBI information is detected, such as WSS.

If a teletext clock run-in is found before line 23 or line 289 for NTSC and (M) PAL, or line 336 for (B, D, G, H, I, N, N_C) PAL, the VBI Teletext Detect status bit is immediately set to “1”. If not found by these lines, the status bit is immediately reset to “0”.

ACCESSING THE TELETEXT DATA

The teletext data must be output as BT.656 ancillary data. The I^2C interface does not have the bandwidth to output teletext information when needed.

Table 8 illustrates the teletext BT.656 ancillary data format and Figure 15 depicts the portion of the incoming teletext signal which is sliced and output as part of the ancillary data stream. The teletext data is present during the horizontal blanking interval after the line containing the teletext information. The actual BT.656 bytes that contain teletext data only contain 4 bits of the actual data packet. Note that only the data packet of Figure 16 is sent as ancillary data; the clock run-in is not included in the data stream.



NOTES:

30. The MSB is bit number: 271 for system C, 279 for system B 525-line and 343 for system B 625-line.
31. The clock run-in is 16 bits wide for both systems and is not included in the BT.656 ancillary data stream.
32. The bit rate is 5.727272 Mbits/s for system B and C on 525/60 systems and 6.9375 and 5.734375 Mbits/second respectively for 625/50 systems.
33. Teletext VBI Video Signal

FIGURE 16. TELETEXT VBI VIDEO SIGNAL

TABLE 8. OUTPUTTING THE SLICED TELETEXT DATA AS BT.656 ANCILLARY DATA

PIXEL INPUT	P15	P14	P13	P12	P11	P10	P9	P8
Preamble	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	1	1
	1	1	1	1	1	1	1	1
Data ID	$\overline{P14}$	ep	1	1	0	1	0	0
Data Block Number	$\overline{P14}$	ep	0	0	0	0	0	1
Data Word Count	$\overline{P14}$	ep	0	1	0	1	1	0
Teletext Data (B, 625-line = 43 bytes) (B, 525-line = 35 bytes) (C = 34 bytes)	$\overline{P14}$	ep	0 = 525-line 1 = 625-line	0 = system B 1 = system C	bit 343	bit 342	bit 341	bit 340
	$\overline{P14}$	ep	0	0	bit 339	bit 338	bit 337	bit 336
	:							
	$\overline{P14}$	ep	0	0	bit 7	bit 6	bit 5	bit 4
	$\overline{P14}$	ep	0	0	bit 3	bit 2	bit 1	bit 0
Reserved	$\overline{P14}$	ep	0	0	0	0	0	0
	$\overline{P14}$	ep	0	0	0	0	0	0
CRC	$\overline{P14}$	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

NOTES:

34. ep = even parity for P8-P13.
35. CRC = Sum of P8-P14 of Data ID through last user data word. Preset to all zeros, carry is ignored.
36. For 525-line system B, bits 280-343 are “0”.
37. For system C, bits 272-343 are “0”.

"RAW" VBI DATA CAPTURE

"Raw" data capture of VBI data during blanked scan lines may be optionally implemented. In this instance, the active line time of blanked scan lines are sampled at the CLK2 rate, and output onto the pixel outputs. This permits software decoding of the VBI data to be done.

The line mask registers specify on which scan lines to generate "raw" VBI data. If the RAW VBI All bit is enabled, all the video lines are treated as raw VBI data, excluding the equalization and serration lines.

The start and end timing of capturing "raw" VBI data on a scan line is determined by the Start and End Raw VBI Registers. This allows the proper capture of "raw" VBI data regardless of the BLANK# output timing for active video.

The blanking level is subtracted from the "raw" VBI data samples, and the result is output onto the pixel outputs.

Note both "sliced" and "raw" VBI data may be available on the same line.

During NTSC operation, the first possible line of VBI data is lines 10 and 272, and the last possible lines are the last blanked scan lines. Lines 1-9 and 264-271 are always blanked.

During PAL (B, D, G, H, I, N, N_C) operation, the first possible line of VBI data are lines 6 and 318, and the last possible lines are the last blanked scan lines. Lines 623-5 and 311-317 are always blanked.

TABLE 9. OUTPUTTING RTCI AS BT.656 ANCILLARY DATA

PIXEL INPUT	P15	P14	P13	P12	P11	P10	P9	P8
Preamble	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	1	1
	1	1	1	1	1	1	1	1
Data ID	$\overline{P14}$	ep	1	1	0	1	0	1
Data Block Number	$\overline{P14}$	ep	0	0	0	0	0	1
Data Word Count	$\overline{P14}$	ep	0	0	0	0	1	1
HPLL Increment	$\overline{P14}$	ep	0	0	0	0	0	0
	$\overline{P14}$	ep	0	0	0	0	0	0
	$\overline{P14}$	ep	0	0	0	0	0	0
	$\overline{P14}$	ep	0	0	0	0	0	0
FSCPLL Increment	$\overline{P14}$	ep	PSW	0	bit 31	bit 30	bit 29	bit 28
	$\overline{P14}$	ep	F2 = 0	F1 = 0	bit 27	bit 26	bit 25	bit 24
	:							
	$\overline{P14}$	ep	0	0	bit 7	bit 6	bit 5	bit 4
	$\overline{P14}$	ep	0	0	bit 3	bit 2	bit 1	bit 0
CRC	$\overline{P14}$	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

NOTES:

38. ep = even parity for P8-P13.

39. CRC = Sum of P8-P14 of Data ID through last user data word. Preset to all zeros, carry is ignored.

During PAL (M) operation, the first possible line of VBI data is lines 7 and 269, and the last possible lines are the last blanked scan lines. Lines 523-6 and 261-268 are always blanked.

Real Time Control Interface

The Real Time Control Interface (RTCI) outputs timing information for a NTSC/PAL encoder as BT.656 ancillary data. This allows the encoder to generate "clean" output video.

RTCI information via BT.656 ancillary data is shown in Table 9. If enabled, this transfer occurs once per line and is completed before the start of the SAV sequence.

The PSW bit is always a "0" for NTSC encoding. During PAL encoding, it indicates the sign of V ("0" = negative; "1" = positive) for that scan line.

Host Interface

All internal registers may be written to or read by the host processor at any time, except for those bits identified as read-only. The bit descriptions for the control registers are listed beginning with Table 10.

The HMP8117 supports the fast-mode (up to 400kbps) I^2C interface consisting of the SDA and SCL pins. The device acts as a slave for receiving and transmitting data over the serial interface. When the interface is not active, SCL and

SDA must be pulled high using external 4kΩ pull-up resistors. The SA input pin determines the slave address for the HMP8117. If the SA pin is pulled low, the address is $1000100x_B$. If the SA pin is pulled high through a 10kΩ pull-up resistor, the address is $1000101x_B$. (This 'x' bit in the address is the I^2C read flag.)

Data is placed on the SDA line when the SCL line is low and held stable when the SCL line is pulled high. Changing the state of the SDA line while SCL is high will be interpreted as either an I^2C bus START or STOP condition as indicated by Figure 18.

During I^2C write cycles, the first data byte after the slave address is treated as the control register sub address and is written into the internal address register. Any remaining data bytes sent during an I^2C write cycle are written to the control registers, beginning with the register specified by the address register as given in the first byte. The address register is then auto-incremented after each additional data byte sent on the I^2C bus during a write cycle. Writes to reserved bits within registers or reserved registers are ignored.

In order to perform a read from a specific control register within the HMP8117, an I^2C bus write must first be performed to properly setup the address register. Then an I^2C bus read can be performed to read from the desired control register(s). As a result of needing the write cycle for a read cycle there are actually two START conditions as shown in Figure 19. The address register is then auto-incremented after each byte read during the I^2C read cycle. Reserved registers return a value of 00_H.

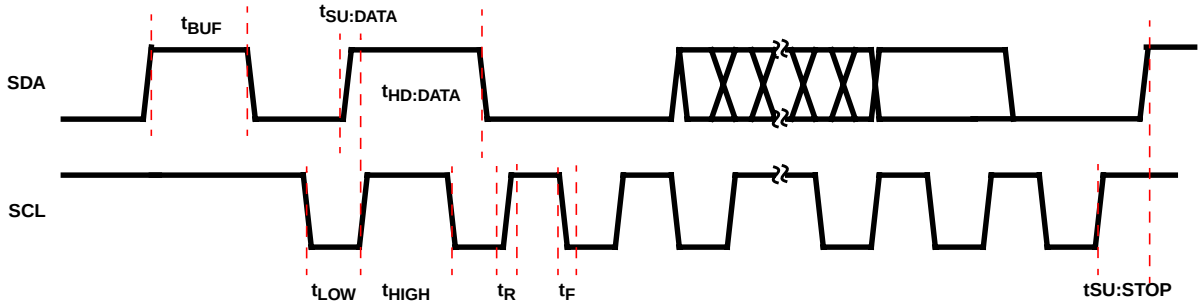


FIGURE 17. I^2C TIMING DIAGRAM

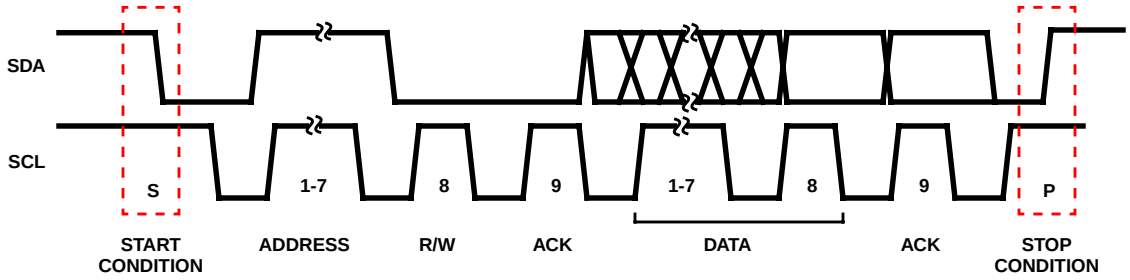


FIGURE 18. I^2C SERIAL DATA FLOW

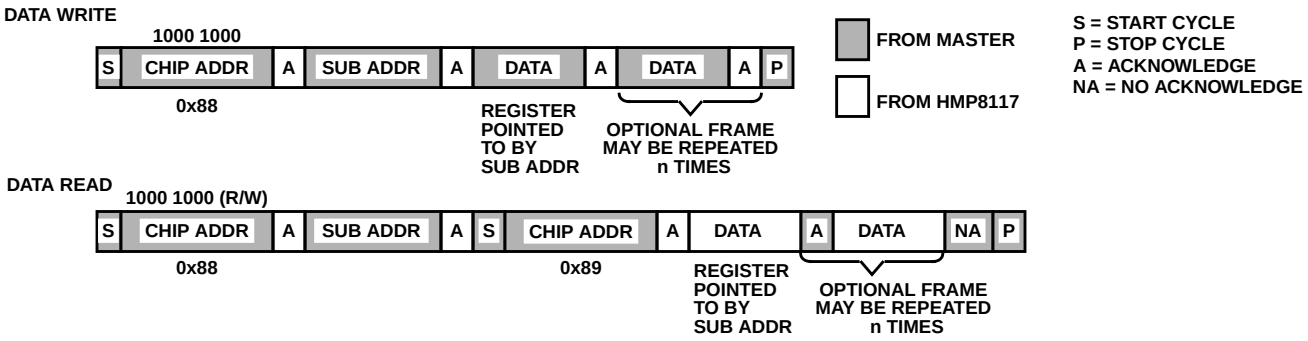


FIGURE 19. REGISTER WRITE/READ FLOW

Control Registers

TABLE 10. CONTROL REGISTER SUMMARY

SUB-ADDRESS	CONTROL REGISTER	RESET/ DEFAULT VALUE	USE VALUE	COMMENTS
00_H	Product ID	16_H or 17_H		Returns last two digits of part number in hex format.
01_H	Input Format	19_H		Defaults to auto-detect of input video standard.
02_H	Output Format	00_H		Defaults to 16-bit YCbCr data format.
03_H	Output Control	00_H	$C0_H$	Set Bits 7-6 to enable data and timing outputs.
04_H	Genlock Control	09_H		Defaults to 27MHz CLK2, Rectangular Pixel Mode
05_H	Analog Input Control	10_H		Defaults to input signal select = CVBS1.
06_H	Color Processing	52_H		
08_H	Luma Processing	04_H		
$0A_H$	Sliced VBI Data Enable	00_H		
$0B_H$	Sliced VBI Data Output	00_H		
$0C_H$	VBI Data Status	00_H		
$0E_H$	Video Status	00_H		
$0F_H$	Interrupt Mask	00_H		
10_H	Interrupt Status	00_H		
11_H	Raw VBI Control	00_H		
12_H	Raw VBI Start Count	$7A_H$		
$14_H/13_H$	Raw VBI Stop Count MSB/LSB	$03_H/4A_H$		
15_H	Raw VBI Line Mask_7_0	FE_H		
16_H	Raw VBI Line Mask_15_8	$1F_H$		
17_H	Raw VBI Line Mask_18_16	00_H		
18_H	Brightness	00_H		
19_H	Contrast	80_H		
$1A_H$	Hue	00_H		

TABLE 10. CONTROL REGISTER SUMMARY (Continued)

SUB-ADDRESS	CONTROL REGISTER	RESET/ DEFAULT VALUE	USE VALUE	COMMENTS
$1B_H$	Saturation	80_H		
$1C_H$	Color Gain Adjust	40_H		
$1D_H$	Video Gain Adjust	80_H		
$1E_H$	Sharpness	10_H		
$1F_H$	Host Control	00_H		Set bit 7 for Soft Reset. Set bit 6 for Power Down.
20_H-23_H	Closed Caption Data Registers	80_H		
24_H-29_H	WSS Data & CRC Registers	00_H		
31_H/30_H	Start H_BLANK MSB/LSB	03_H/$4A_H$	Table 3	$\overline{\text{BLANK}}$ programming changes for each video standard.
32_H	End H_BLANK	$7A_H$	Table 3	(same as above)
34_H/33_H	Start V_BLANK MSB/LSB	01_H/02_H	Table 3	(same as above)
35_H	End V_BLANK	12_H	Table 3	(same as above)
36_H	End HSYNC	30_H	Table 3	(same as above)
37_H	HSYNC Detect Window	20_H	90_H	A wider window tolerates poorly timed video sources.
41_H	MV Control	26_H		
42_H	Reserved	00_H	30_H	Set bits 5-4 to 11_B for optimum performance.
50_H	Programmable Fractional Gain	$0C_H$	21_H	A slower PFG improves AGC stability.
51_H	MV Stripe Gate	14_H		
52_H	Reserved	02_H	22_H	Set bit 5 to “1” for optimum performance.
53_H	AGC Hysteresis	00_H	$F0_H$	Larger hysteresis improves AGC stability.
$7F_H$	Device Revision	01_H		Production baseline revision is 01_H.
Sub-Addresses: 40_H, 43_H-$4F_H$ are reserved. Reads from these registers may return non-zero values.				
Sub-Addresses: 07_H, 09_H, $0D_H$, $2A_H$-$2F_H$, 38_H-$3F_H$ and 54_H-$7E_H$ are unused. Reads from these registers return 00_H. Writes are ignored.				

TABLE 11. PRODUCT ID REGISTER

SUB ADDRESS = 00_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Product ID	This 8-bit register specifies the last two digits of the product number. Data written to this read-only register is ignored.	17_H

TABLE 12. INPUT FORMAT REGISTER.

SUB ADDRESS = 01_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Reserved		0_B
6-5	Video Timing Standard	These bits are read only unless bit 4 = “0”. 00 = (M) NTSC 01 = (B, D, G, H, I, N) PAL 10 = (M) PAL 11 = Combination (N) PAL; also called (N_C) PAL	00_B
4	Auto Detect Video Standard	0 = Manual selection of video timing standard 1 = Auto detect of video timing standard	1_B
3	Setup Select	Typically, this bit should be a “1” during (M) NTSC and (M, N) PAL operation. Otherwise, it should be a “0”. 0 = Video source has a 0 IRE blanking pedestal 1 = Video source has a 7.5 IRE blanking pedestal	1_B
2-1	Reserved		00_B

TABLE 12. INPUT FORMAT REGISTER.

SUB ADDRESS = 01_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
0	Adaptive Sync Slice Enable	This bit specifies whether to use fixed or adaptive sync slicing. Adaptive sync slicing automatically determines the midpoint of the sync amplitude to determine timing. 0 = Fixed sync slicing 1 = Adaptive sync slicing	1_B

TABLE 13. OUTPUT FORMAT REGISTER.

SUB ADDRESS = 02_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-5	Output Color Format	000 = 16-bit 4:2:2 YCbCr100 = 16-bit RGB 001 = 8-bit 4:2:2 YCbCr101 = reserved 010 = 8-bit parallel BT.656110 = reserved 011 = 15-bit RGB111 = reserved	000_B
4-3	RGB Gamma Select	These bits are ignored except during RGB output modes. 00 = Linear RGB (gamma of input source = 2.2) 01 = Linear RGB (gamma of input source = 2.8) 10 = Gamma-corrected RGB (gamma = gamma of input source) 11 = reserved	00_B
2-1	Output Color Select	00 = Normal operation10 = Output black field 01 = Output blue field11 = Output 75% color bars	00_B
0	Reserved	Set to “0” for proper operation. Vertical Pixel Siting control is not supported.	0_B

TABLE 14. OUTPUT CONTROL REGISTER.

SUB ADDRESS = 03_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Video Data Output Enable	This bit is used to enable the P0-P15 outputs. 0 = Outputs 3-stated. 1 = Outputs enabled	0_B
6	Video Timing Output Enable	This bit is used to enable the $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$, FIELD, $\overline{\text{VBIVALID}}$, $\overline{\text{DVALID}}$, and $\overline{\text{INTREQ}}$ outputs. 0 = Outputs 3-stated. 1 = Outputs enabled	0_B
5	FIELD Polarity	0 = Active low (low during odd fields). 1 = Active high (high during odd fields)	0_B
4	$\overline{\text{BLANK}}$ Polarity	0 = Active low (low during blanking). 1 = Active high (high during blanking)	0_B
3	$\overline{\text{HSYNC}}$ Polarity	0 = Active low (low during horizontal sync). 1 = Active high (high during horizontal sync)	0_B
2	$\overline{\text{VSYNC}}$ Polarity	0 = Active low (low during vertical sync). 1 = Active high (high during vertical sync)	0_B
1	$\overline{\text{DVALID}}$ Polarity	0 = Active low (low during valid pixel data). 1 = Active high (high during valid pixel data)	0_B
0	$\overline{\text{VBIVALID}}$ Polarity	0 = Active low (low during VBI data). 1 = Active high (high during VBI data)	0_B

TABLE 15. GENLOCK CONTROL REGISTER

SUB ADDRESS = 04_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Aspect Ratio Mode	0 = Rectangular (BT.601) pixels 1 = Square pixels	0_B
6	Freeze Output Timing Enable	Setting this bit to a “1” freezes the output timing at the end of the field. Resetting this bit to a “0” resumes normal operation at the start of the next field. 0 = Normal operation 1 = Freeze output timing	0_B
5	$\overline{\text{DVALID}}$ Duty Cycle Control (DVLD_DCYC)	This bit is ignored during the 8-bit YCbCr and BT.656 output modes. During 16-bit YCbCr, 15-bit RGB, or 16-bit RGB output modes, this bit is defined as: 0 = $\overline{\text{DVALID}}$ has 50/50 duty cycle at the pixel output data rate 1 = $\overline{\text{DVALID}}$ goes active based on line-lock. This will cause $\overline{\text{DVALID}}$ to not have a 50/50 duty cycle. This bit is intended to be used in maintaining backward compatibility with the HMP8112A $\overline{\text{DVALID}}$ output timing.	0_B
4	$\overline{\text{DVALID}}$ Line Timing Control (DVLD_LTC)	During 16-bit YCbCr, 15-bit RGB, or 16-bit RGB output modes, this bit is defined as: 0 = $\overline{\text{DVALID}}$ present only during active video time on active scan lines 1 = $\overline{\text{DVALID}}$ present the entire scan line time on all scan lines During the 8-bit YCbCr and BT.656 output modes, this bit defines the $\overline{\text{DVALID}}$ output as: 0 = Normal timing 1 = $\overline{\text{DVALID}}$ signal ANDed with CLK2	0_B
3	Missing $\overline{\text{HSYNC}}$ Detect Select	This bit specifies the number of missing horizontal sync pulses before entering horizontal lock acquisition mode. 0 = 12 pulses 1 = 1 pulse	1_B
2	Missing $\overline{\text{VSYNC}}$ Detect Select	This bit specifies the number of missing vertical sync pulses before entering vertical lock acquisition mode. 0 = 3 pulses 1 = 1 pulse	0_B
1-0	CLK2 Frequency	This bit indicates the frequency of the CLK2 input clock. 00 = 24.54MHz10 = 29.5MHz 01 = 27.0MHz11 = Reserved	01_B

TABLE 16. ANALOG INPUT CONTROL REGISTER

SUB ADDRESS = 05_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-6	Lock Loss Video Gain Select	If bits 5-4 do not equal “01”, these bits indicate what mode the AGC circuitry will be after loss of sync. If bits 5-4 equal “01”, these bits are ignored. 00 = Automatic gain control: bits 5-4 will be reset to “01” 01 = Maintain fixed gain: bits 5-4 will not be changed 10 = Normal AGC switching to fixed gain after lock achieved: bits 5-4 will not be reset to “01” unless they indicated “freeze automatic gain control” 11 = reserved	00_B
5-4	Video Gain Control Select	00 = Fixed 1x gain 01 = Automatic gain control 10 = Fixed gain control. (Use gain factor from Video Gain Adjust register $1D_H$.) 11 = Freeze automatic gain control	01_B
3	Digital Anti-Alias Filter Control	0 = Internal digital anti-alias filter is active. 1 = Internal digital anti- alias filter is bypassed. (Not Recommended)	0_B
2-0	Video Signal Input Select	000 = CVBS1 001 = CVBS2 010 = CVBS3 011 = S-video 1XX = reserved	000_B

TABLE 17. COLOR PROCESSING REGISTER

SUB ADDRESS = 06_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-6	Digital Color Gain Control Select	00 = No gain control (gain = 1x) 01 = Automatic gain control 10 = Fixed gain control. (Use gain factor from Color Gain Adjust register $1C_H$.) 11 = Freeze automatic gain control	01_B
5-4	Color Killer Select	00 = Force color on 01 = Enable color killer 10 = reserved 11 = Force color off	01_B
3-2	Color Coring Select	Coring may be used to reduce low-level noise in the CbCr signals. 00 = No coring 01 = 1 code coring 10 = 2 code coring 11 = 3 code coring	00_B
1	Contrast Control Select	This bit specifies whether the contrast control affects just the Y data (“0”) or both the Y and CbCr data (“1”). To avoid color shifts when changing contrast, this bit should be a “1”. 0 = Contrast controls only Y data 1 = Contrast controls Y and CbCr data	1_B
0	Color Low-Pass Filter Select	This bit selects the bandwidth of the CbCr data. 0 = 850kHz 1 = 1.5MHz	0_B

TABLE 18. LUMA PROCESSING REGISTER

SUB ADDRESS = 08_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-6	Y Filtering Select	The chroma trap filter may be used to remove any residual color subcarrier information from the Y channel. During S-video operation, it should be disabled. During PAL operation, it should be enabled. The 3MHz low-pass filter may be used to remove high-frequency noise. 00 = No filtering 01 = Enable chroma trap filter 10 = Enable 3.0MHz low-pass filter 11 = reserved	00_B
5-4	Black Level Y Coring Select	Coring may be used to reduce low-level noise around black in the Y signal. 00 = No coring 01 = 1 code coring 10 = 2 code coring 11 = 3 code coring	00_B
3-2	High Frequency Y Coring Select	Coring may be used to reduce high-frequency low-level noise in the Y signal. 00 = No coring 01 = 1 code coring 10 = 2 code coring 11 = 3 code coring	01_B
1-0	Sharpness Frequency Select	Specifies the amount of sharpness to be applied per the Sharpness Adjust register $1E_H$. 00 = Bypass sharpness control10 = Maximum gain at color F_{SC} 01 = Maximum gain at 2.6MHz11 = reserved	00_B

TABLE 19. SLICED VBI DATA ENABLE REGISTER

SUB ADDRESS = $0A_H$			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-6	Sliced Closed Captioning Enable	00 = Closed caption disabled 01 = Closed caption enabled for odd fields: line 21 for NTSC, line 18 for (M) PAL, or line 22 for (B, D, G, H, I, N, N_C) PAL 10 = Closed caption enabled for even fields: line 284 for NTSC, line 281 for (M) PAL, or line 335 for (B, D, G, H, I, N, N_C) PAL 11 = Closed caption enabled for both odd and even fields	00_B
5-4	Sliced WSS Enable	00 = WSS disabled 01 = WSS enabled for odd fields: line 20 for NTSC; line 17 for (M) PAL, or line 23 for (B, D, G, H, I, N, N_C) PAL 10 = WSS enabled for even fields: line 283 for NTSC, line 280 for (M) PAL, or line 336 for (B, D, G, H, I, N, N_C) PAL 11 = WSS enabled for both odd and even fields	00_B
3-2	Sliced Teletext Enable	00 = Teletext disabled10 = Teletext system C enabled 01 = Teletext system B enabled11 = Teletext system D enabled	00_B
1-0	Reserved		00_B

TABLE 20. SLICED VBI DATA OUTPUT REGISTER

SUB ADDRESS = $0B_H$			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Sliced Closed Caption BT.656 Output Enable	If set to “1”, this bit enables output of sliced closed captioning via BT.656 ancillary data. Closed captioning must be enabled by the Sliced VBI Data Enable register $0A_H$. Access via the I^2C interface is always available.	0_B
6	Sliced WSS BT.656 Output Enable	If set to “1”, this bit enables output of sliced WSS via BT.656 ancillary data. WSS must be enabled by the Sliced VBI Data Enable register $0A_H$. Access via the I^2C interface is always available.	0_B
5	Sliced Teletext BT.656 Output Enable	If set to “1”, this bit enables output of sliced teletext via BT.656 ancillary data. Teletext data is not available via the I^2C interface.	0_B
4-1	Reserved		0000_B
0	RTCI BT.656 Output Enable	If set to “1”, this bit enables output of RTCI data as BT.656 ancillary data.	0_B

TABLE 21. VBI DATA STATUS REGISTER

SUB ADDRESS = $0C_H$			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	CC Odd Field Detect Status	This bit is read-only. Data written to this bit is ignored. If set to “1”, Closed Captioning (CC) data is detected on the odd field.	0_B
6	CC Even Field Detect Status	This bit is read-only. Data written to this bit is ignored. If set to “1”, Closed Captioning (CC) data is detected on the even field.	0_B
5	WSS Odd Field Detect Status	This bit is read-only. Data written to this bit is ignored. If set to “1”, Wide Screen Signalling (WSS) data is detected on the odd field.	0_B
4	WSS Even Field Detect Status	This bit is read-only. Data written to this bit is ignored. If set to “1”, Wide Screen Signalling (WSS) data is detected on the even field.	0_B
3	VBI Teletext Detect Status	This bit is read-only. Data written to this bit is ignored. If set to “1”, Teletext data is detected during the vertical blanking interval.	0_B
2-0	Reserved		000_B

TABLE 22. VIDEO STATUS REGISTER

SUB ADDRESS = $0E_H$			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Vertical Lock Status	This bit is read-only. Data written to this bit is ignored. If set to “1”, the decoder is vertically locked to the input signal.	0_B
6	Horizontal Lock Status	This bit is read-only. Data written to this bit is ignored. If set to “1”, the decoder is horizontally locked to the input signal.	0_B
5	Color Lock Status	This bit is read-only. Data written to this bit is ignored. If set to “1”, the decoder is chroma locked to the input signal.	0_B
4	Input Video Detect Status	This bit is read-only. Data written to this bit is ignored. If set to “1”, video is detected on the input signal.	0_B
3-1	MV Detection Status	These bits are read-only. Data written to this bit is ignored. 000_B = No MV present 001_B = PSP present, No Stripes 010_B = PSP present, 2-Line Stripes 011_B = PSP present, 4-line Stripes 100_B = reserved 101_B = reserved 110_B = No PSP present, 2-line Stripes (invalid MV scheme, may indicate false detection) 111_B = No PSP present, 4-line Stripes (invalid MV scheme, may indicate false detection)	000_B
0	Auto Detect Video Standard Status	This bit is read-only. Data written to this bit is ignored. If set to “1”, the decoder determined the video standard on the input signal. This bit is enabled by the Input Format Register 01_H bit 4.	0_B

TABLE 23. INTERRUPT MASK REGISTER

SUB ADDRESS = $0F_H$			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Genlock Loss Interrupt Mask	If set to “1”, an interrupt is enabled for the loss of genlock.	0_B
6	Input Signal Loss Interrupt Mask	If set to “1”, an interrupt is enabled for the loss of input video signal.	0_B
5	Closed Caption Interrupt Mask	If set to “1”, an interrupt is enabled for new data in the closed caption data registers.	0_B
4	WSS Interrupt Mask	If set to “1”, an interrupt is enabled for new data in the WSS data registers.	0_B
3	Teletext Interrupt Mask	If set to “1”, an interrupt is enabled for the detection of teletext data in the current field.	0_B
2	MV Interrupt Mask	If set to “1”, an interrupt is enabled for a change in the MV Detection Status Register $0E_H$.	0_B
1	Auto Detect Video Standard Interrupt Mask	If set to “1”, an interrupt is enabled for the successful auto detection of a video standard.	0_B
0	Vertical Sync Interrupt Mask	If set to “1”, an interrupt is enabled for the start of a new field.	0_B

TABLE 24. INTERRUPT STATUS REGISTER

SUB ADDRESS = 10_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Genlock Loss Interrupt Status	If set to “1”, this bit indicates the interrupt request was due to a loss of genlock. To clear the interrupt request, a “1” must be written to this bit.	0_B
6	Input Signal Loss Interrupt Status	If set to “1”, this bit indicates the interrupt request was due to a loss of input video signal. To clear the interrupt request, a “1” must be written to this bit.	0_B
5	Closed Caption Interrupt Status	If set to “1”, this bit indicates the interrupt request was due to new data in the closed caption data registers. To clear the interrupt request, a “1” must be written to this bit.	0_B
4	WSS Interrupt Status	If set to “1”, this bit indicates the interrupt request was due to new data available in the WSS data registers. To clear the interrupt request, a “1” must be written to this bit.	0_B
3	Teletext Interrupt Status	If set to “1”, this bit indicates the interrupt request was due to the detection of teletext data in the current field. To clear the interrupt request, a “1” must be written to this bit.	0_B
2	MV Interrupt Status	If set to “1”, this bit indicates the interrupt request was due to a change in the MV Detection Status of register $0E_H$. To clear the interrupt request, a “1” must be written to this bit.	0_B
1	Auto Detect Video Standard Interrupt Status	If set to “1”, this bit indicates the interrupt request was due to the successful auto detection of a video standard. To clear the interrupt request, a “1” must be written to this bit.	0_B
0	Vertical Sync Interrupt Status	If set to “1”, this bit indicates the interrupt request was due to the start of a new field. To clear the interrupt request, a “1” must be written to this bit.	0_B

TABLE 25. RAW VBI CONTROL REGISTER

SUB ADDRESS = 11_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-4	Reserved		0000_B
3	RAW Preamble Enable	If set to “1”, enables a four byte preamble in the RAW VBI data stream. The preamble format is FF_H, CNT1, CNT2 and 00H, where: CNT1: Bit 7 = even parity bar, Bit 6 = even parity[5-0], Bit 5 = 0, Bit 4 = Field (0=Odd, 1=Even), Bits 3 -0 =Linecount[8-4]. CNT2: Bit 7 = even parity bar, Bit 6 = even parity [5-0], Bits 5-4 = 00 Bits 3-0 = Linecount[3-0].	0_B
2	RAW VBI All	If set to “1”, all the video lines (full field) are converted to RAW VBI data. If set to “0”, only the lines enabled by the RAW VBI LINE MASK registers are converted to RAW VBI data.	0_B
1	RAW VBI Even Field	If set to “1”, even field lines are converted to RAW VBI data as specified by the RAW VBI All bit and the RAW VBI LINE MASK registers. If set to “0”, the even field lines are excluded from the RAW VBI data stream.	0_B
0	RAW VBI Odd Field	If set to “1”, odd field lines are converted to RAW VBI data as specified by the RAW VBI All bit and the RAW VBI LINE MASK registers. If set to “0”, the odd field lines are excluded from the RAW VBI data stream.	0_B

TABLE 26. RAW VBI START COUNT REGISTER

SUB ADDRESS = 12_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Raw VBI Start Count	Specifies the start of the raw VBI data sampling window in two CLK2 period steps from the leading edge of HSYNC.	$7A_H$

TABLE 27. RAW VBI STOP COUNT LSB REGISTER

SUB ADDRESS = 13_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Raw VBI Stop Count LSB	This 8-bit register is cascaded with Raw VBI Stop Count MSB (below) to form a 10-bit stop count value. The stop count specifies the end of the raw VBI data sampling window in two CLK2 period steps from the leading edge of HSYNC.	$4A_H$

TABLE 28. RAW VBI STOP COUNT MSB REGISTER

SUB ADDRESS = 14_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-2	Reserved		000000_B
1-0	Raw VBI Stop Count MSB	This 2-bit register is cascaded with Raw VBI Stop Count LSB (above) to form a 10-bit stop count value. The stop count specifies the end of the raw VBI data sampling window in two CLK2 period steps from the leading edge of HSYNC.	11_B

TABLE 29. RAW VBI LINE MASK_7_0 REGISTER

SUB ADDRESS = 15_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Raw VBI Line Mask_7_0	A “1” in each bit position enables raw VBI capture for a corresponding input video line. Refer to Table 32 below.	FE_H

TABLE 30. RAW VBI LINE MASK_15_8 REGISTER

SUB ADDRESS = 16_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Raw VBI Line Mask_15_8	A “1” in each bit position enables raw VBI capture for a corresponding input video line. Refer to Table 32 below.	$1F_H$

TABLE 31. RAW VBI LINE MASK_18_16 REGISTER

SUB ADDRESS = 17_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-3	Reserved		00000_B
2-0	Raw VBI Line Mask_18_16	A “1” in each bit position enables raw VBI capture for a corresponding input video line. Refer to Table 32 below.	000_B

TABLE 32. RAW VBI MASK DEFINITIONS

MASK (Register = Default)	MASK_18_16 (Reg. 17_H)			MASK_15_8 (Register 16_H)								MASK_7_0 (Register 15_H)							
REGISTER BIT	**2**	**1**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Mask Bit	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NTSC (Odd) Line#	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9
NTSC (Even) Line#	290	289	288	287	286	285	284	283	282	281	280	279	278	277	276	275	274	273	272
PAL (Odd) Line#	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5
PAL (Even) Line#	336	335	334	333	332	331	330	329	328	327	326	325	324	323	322	321	320	319	318

TABLE 33. BRIGHTNESS REGISTER

SUB ADDRESS = 18_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Reserved		0_B
6-0	Brightness Adjust	These bits control the brightness. They may have a value of +63 (“011 1111”) to -64 (“100 0000”), with positive values increasing brightness. A value of 0 (“000 0000”) has no effect on the data.	0000000_B

TABLE 34. CONTRAST REGISTER

SUB ADDRESS = 19_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Contrast Adjust	These bits control the contrast. They may have a value of 0x (“0000 0000”) to 1.992x (“1111 1111”). A value of 1x (“1000 0000”) has no effect on the data.	80_H

TABLE 35. HUE REGISTER

SUB ADDRESS = $1A_H$			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Hue Adjust	These bits control the color hue. They may have a value of +30 degrees (“0111 1111”) to -30 degrees (“1111 1111”). A value of 0 degrees (“0000 0000”) has no effect on the color data.	00_H

TABLE 36. SATURATION REGISTER

SUB ADDRESS = $1B_H$			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Saturation Adjust	These bits control the color saturation. They may have a value of 0x (“0000 0000”) to 1.992x (“1111 1111”). A value of 1x (“1000 0000”) has no effect on the color data. A value of 0x (“0000 0000”) disables the color information.	80_H

TABLE 37. COLOR GAIN ADJUST REGISTER

SUB ADDRESS = $1C_H$			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Color Gain Adjust	These bits control the amount of digital gain applied to the color difference (CbCr) signals. They may have a value of 0.5x (“0010 0000”) to 3.98x (“1111 1111”). A value of 1x (“0100 0000”) has no effect on the data. This register enabled by the selection of “fixed gain control” mode in the Color Processing register 06_H.	40_H

TABLE 38. VIDEO GAIN ADJUST REGISTER

SUB ADDRESS = $1D_H$			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Video Gain Adjust	This register is enabled by the selection of “fixed gain control” mode in the Analog Input Control register 05_H bits 7-4. The value of this register selects a combined analog attenuation and a digital gain factor which is applied to both Luma and Chroma input channels. The gain factor is selected from nonlinear lookup table and may range in value from 0.5x (CE_H) to 1.99x (33_H). Refer to Table 39 below. The Register Values in *italics* below mark the approximate analog attenuation ladder switching points.	80_H

TABLE 39. VIDEO GAIN REGISTER LOOKUP TABLE

Video Gain	Reg. Value	Video Gain	Reg. Value	Video Gain	Reg. Value	Video Gain	Reg. Value	Video Gain	Reg. Value	Video Gain	Reg. Value
0.50	206/CEH	0.67	$153/99_H$	0.84	$123/7B_H$	1.03	$100/64_H$	1.23	$83/53_H$	1.55	$66/42_H$
0.51	$202/CA_H$	0.68	$151/97_H$	0.85	$121/79_H$	1.04	$99/63_H$	1.25	$82/52_H$	1.57	$65/41_H$
0.52	$197/C5_H$	*0.69*	*150/96H*	0.86	$119/77_H$	1.05	$98/62_H$	1.27	$81/51_H$	1.59	$64/40_H$
0.53	$193/C1_H$	0.70	$147/93_H$	0.87	$118/76_H$	1.06	$97/61_H$	1.28	$80/50_H$	1.63	$63/3F_H$
0.54	$191/BF_H$	0.71	$145/91_H$	0.88	$117/75_H$	1.07	$96/60_H$	1.30	$79/4F_H$	1.65	$62/3E_H$
0.55	$187/BB_H$	0.72	$143/8F_H$	*0.89*	*115/73H*	1.08	$95/5F_H$	1.31	$78/4E_H$	1.67	$61/3D_H$
0.56	$183/B7_H$	0.73	$141/8D_H$	0.90	$114/72_H$	1.09	$94/5E_H$	*1.33*	*77/4DH*	1.70	$60/3C_H$
0.57	$180/B4_H$	0.74	$139/8B_H$	0.91	$113/71_H$	1.10	$93/5D_H$	1.34	$76/4C_H$	*1.73*	*59/3BH*
0.58	$178/B2_H$	0.75	$137/89_H$	0.92	$111/6F_H$	1.12	$92/5C_H$	1.37	$75/4B_H$	1.76	$58/3A_H$
0.59	$174/AE_H$	0.76	$136/88_H$	0.94	$110/6E_H$	1.13	$91/5B_H$	1.38	$74/4A_H$	1.79	$57/39_H$
0.60	$171/AB_H$	0.77	$134/86_H$	0.95	$109/6D_H$	1.14	$90/5A_H$	1.40	$73/49_H$	1.82	$56/38_H$
0.61	$169/A9_H$	*0.78*	*132/84H*	0.96	$107/6B_H$	1.15	$89/59_H$	1.42	$72/48_H$	1.86	$55/37_H$
0.62	$167/A7_H$	0.79	$130/82_H$	0.97	$106/6A_H$	*1.16*	*88/58H*	1.44	$71/47_H$	1.89	$54/36_H$
0.63	$164/A4_H$	0.80	$128/80_H$	0.98	$104/68_H$	1.18	$87/57_H$	1.46	$70/46_H$	1.93	$53/35_H$
0.64	$161/A1_H$	0.81	$126/7E_H$	1.00	$103/67_H$	1.20	$86/56_H$	1.48	$69/45_H$	1.97	$52/34_H$
0.65	$159/9F_H$	0.82	$125/7D_H$	1.01	$102/66_H$	1.21	$85/55_H$	*1.51*	*68/44H*	*1.99*	*51/33H*
0.66	$156/9C_H$	0.83	$124/7C_H$	*1.02*	*101/65H*	1.22	$84/54_H$	1.52	$67/43_H$		

TABLE 40. SHARPNESS ADJUST REGISTER

SUB ADDRESS = $1E_H$			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-6	Reserved		00_B
5-0	Sharpness Adjust	Specifies the amount of high frequency gain control for luminance signals (either 2.6MHz or F_{SC}), as determined by the Luma Processing register 08_H. The gain ranges from +12dB (11 1111_B) to -12dB (00 0100_B). A value of 0dB (“01 0000”) has no effect on the data.	010000_B

TABLE 41. HOST CONTROL REGISTER

SUB ADDRESS = $1F_H$			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Software Reset	When this bit is set to 1, the entire device except the I^2C bus is reset to a known state exactly like the $\overline{\text{RESET}}$ input going active. The software reset will initialize all register bits to their reset state. Once set this bit is self clearing. This bit is cleared on power-up by the external $\overline{\text{RESET}}$ pin.	0_B
6	Power Down	When this bit is set to a 1, the entire device is shut down except the I^2C bus by gating off the clock. For normal decoding operations this bit should be set to a 0.	0_B
5	Closed Caption Odd Field Read Status	This bit is read-only. Data written to this bit is ignored. The bit is cleared when the caption data has been read out via the I^2C interface or as BT.656 ancillary data. 0 = No new caption data 1 = Caption_ODD_A and Caption_ODD_B data registers contain new data.	0_B
4	Closed Caption Even Field Read Status	This bit is read-only. Data written to this bit is ignored. The bit is cleared when the caption data has been read out via the I^2C interface or as BT.656 ancillary data. 0 = No new caption data 1 = Caption_EVEN_A and Caption_EVEN_B data registers contain new data.	0_B
3	WSS Odd Field Read Status	This bit is read-only. Data written to this bit is ignored. The bit is cleared when the WSS data has been read out via the I^2C interface or as BT.656 ancillary data. 0 = No new WSS data 1 = WSS_ODD_A and WSS_ODD_B data registers contain new data.	0_B
2	WSS Even Field Read Status	This bit is read-only. Data written to this bit is ignored. The bit is cleared when the WSS data has been read out via the I^2C interface or as BT.656 ancillary data. 0 = No new WSS data 1 = WSS_EVEN_A and WSS_EVEN_B data registers contain new data.	0_B
1-0	Reserved		00_B

TABLE 42. CLOSED CAPTION_ODD_A DATA REGISTER

SUB ADDRESS = 20_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Odd Field Caption Data	If odd field captioning is enabled and present, this register is loaded with the first eight bits of caption data on line 18, 21, or 22. Bit 0 corresponds to the first bit of caption information. Data written to this register is ignored.	80_H

TABLE 43. CLOSED CAPTION_ODD_B DATA REGISTER

SUB ADDRESS = 21_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
15-8	Odd Field Caption Data	If odd field captioning is enabled and present, this register is loaded with the second eight bits of caption data on line 18, 21, or 22. Data written to this register is ignored.	80_H

TABLE 44. CLOSED CAPTION_EVEN_A DATA REGISTER

TABLE 45. SUB ADDRESS = 22_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Even Field Caption Data	If even field captioning is enabled and present, this register is loaded with the first eight bits of caption data on line 281, 284, or 335. Bit 0 corresponds to the first bit of caption information. Data written to this register is ignored.	80_H

TABLE 46. CLOSED CAPTION_EVEN_B DATA REGISTER

SUB ADDRESS = 23_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
15-8	Even Field Caption Data	If even field captioning is enabled and present, this register is loaded with the second eight bits of caption data on line 281, 284, or 335. Data written to this register is ignored.	80_H

TABLE 47. WSS_ODD_A DATA REGISTER

SUB ADDRESS = 24_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Odd Field WSS Data	If odd field WSS is enabled and present, this register is loaded with the first eight bits of WSS information on line 17, 20, or 23. Bit 0 corresponds to the first bit of WSS information. Data written to this register is ignored.	00_H

TABLE 48. WSS_ODD_B DATA REGISTER

SUB ADDRESS = 25_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
15-14	Reserved		00_B
13-8	Odd Field WSS Data	If odd field WSS is enabled and present, this register is loaded with the second six bits of WSS information on line 17, 20, or 23. Data written to this register is ignored.	000000_B

TABLE 49. WSS_CRC_ODD DATA REGISTER

SUB ADDRESS = 26_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-6	Reserved		00_B
5-0	Odd Field WSS CRC Data	If odd field WSS is enabled and present during NTSC operation, this register is loaded with the six bits of CRC information on line 20. It is always a “000000” during PAL operation. Data written to this register is ignored.	000000_B

TABLE 50. WSS_EVEN_A DATA REGISTER

SUB ADDRESS = 27_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Even Field WSS Data	If even field WSS is enabled and present, this register is loaded with the first eight bits of WSS information on line 280, 283, or 336. Bit 0 corresponds to the first bit of WSS information. Data written to this register is ignored.	00_H

TABLE 51. WSS_EVEN_B DATA REGISTER

SUB ADDRESS = 28_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
15-14	Reserved		00_B
13-8	Even Field WSS Data	If even field WSS is enabled and present, this register is loaded with the second six bits of WSS information on line 280, 283, or 336. Data written to this register is ignored.	000000_B

TABLE 52. WSS_CRC_EVEN DATA REGISTER

SUB ADDRESS = 29_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-6	Reserved		00_B
5-0	Even Field WSS CRC Data	If even field WSS is enabled and present during NTSC operation, this register is loaded with the six bits of CRC information on line 283. It is always a “000000” during PAL operation. Data written to this register is ignored.	000000_B

TABLE 53. START H_BLANK LSB REGISTER

SUB ADDRESS = 30_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Assert $\overline{BLANK}$ Output Signal	This 8-bit register is cascaded with Start H_BLANK High Register to form a 10-bit start horizontal blank REGISTER. It specifies the horizontal count (in 1x clock cycles) at which to assert $\overline{BLANK}$ each scan line. Bit 0 is always a “0”, so the start of horizontal blanking may only be done with two pixel resolution. The leading edge of $\overline{HSYNC}$ is count 000_H.	$4A_H$

TABLE 54. START H_BLANK MSB REGISTER

SUB ADDRESS = 31_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
15-10	Reserved		000000_B
9-8	Assert $\overline{BLANK}$ Output Signal	This 2-bit register is cascaded with Start H_BLANK Low Register to form a 10-bit start horizontal blank register. It specifies the horizontal count (in 1x clock cycles) at which to assert $\overline{BLANK}$ each scan line. The leading edge of $\overline{HSYNC}$ is count 000_H.	11_B

TABLE 55. END H_BLANK REGISTER

SUB ADDRESS = 32_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Negate $\overline{BLANK}$ Output Signal	This 8-bit register specifies the horizontal count (in 1x clock cycles) to negate $\overline{BLANK}$ each scan line. For proper operation, bit 0 must always be set to “0”; therefore, the end of horizontal blanking may only set with two pixel resolution. If bit 0 is set to “1”, the chroma/luma output data may be swapped. The leading edge of $\overline{HSYNC}$ is count 000_H.	$7A_H$

TABLE 56. START V_BLANK LSB REGISTER

SUB ADDRESS = 33_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Assert $\overline{BLANK}$ Output Signal	This 8-bit register is cascaded with Start V_BLANK High Register to form a 9-bit start vertical blank register. It specifies the line number to assert $\overline{BLANK}$ each field. For NTSC operation, it occurs on line (n + 5) on odd fields and line (n + 268) on even fields. For PAL operation, it occurs on line (n + 5) on odd fields and line (n + 318) on even fields.	02_H

TABLE 57. START V_BLANK MSB REGISTER

SUB ADDRESS = 34_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
15-9	Reserved		0000000_B
8	Assert $\overline{BLANK}$ Output Signal	This 1-bit register is cascaded with Start V_BLANK Low Register to form a 9-bit start vertical blank register.	1_B

TABLE 58. END V_BLANK REGISTER

SUB ADDRESS = 35_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Negate $\overline{\text{BLANK}}$ Output Signal	This 8-bit register specifies the line number to negate $\overline{\text{BLANK}}$ each field. For NTSC operation, it occurs on line (n + 5) on odd fields and line (n + 268) on even fields. For PAL operation, it occurs on line (n + 5) on odd fields and line (n + 318) on even fields.	12_H

TABLE 59. END HSYNC REGISTER

SUB ADDRESS = 36_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Negate $\overline{\text{HSYNC}}$ Output Signal	This 8-bit register specifies the horizontal count at which to negate $\overline{\text{HSYNC}}$ each scan line. Values may range from 0 (0000 0000) to 510 (1111 1111) CLK2 cycles. The leading edge of $\overline{\text{HSYNC}}$ is count 00_H.	30_H

TABLE 60. HSYNC DETECT WINDOW REGISTER

SUB ADDRESS = 37_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Horizontal Sync Detect Window	This 8-bit register specifies the width of the timing window (in 1x clock samples) for the digital PLL to accept horizontal sync pulses in each line. The window is centered about where the horizontal sync pulse should be located. If the horizontal sync pulse falls inside the window, the digital PLL maintains normal lock timing. If the horizontal sync pulse falls outside this window, the digital PLL will to enter the horizontal lock acquisition mode based on the current setting for bits 3-2 of register 04_H. Recommend changing this register to 90_H following reset in order to widen the window for poorly timed input video sources.	20_H (Use 90_H)

TABLE 61. MV CONTROL

SUB ADDRESS = 41_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	MV Stripe Detection and Bypass Enable	Set to “1” to enable the detection and bypass of the MV Color Striping component. If this bit is not enabled and the MV Color Striping component exists on the input signal, artifacts will be clearly visible as horizontal streaks in the output data. This bit must be enabled for the MV Detection Status of register $0E_H$ to be updated.	0_B
6	MV PSP Detection Enable	Set to “1” to enable detection of the MV Pseudo Sync Pulse (PSP) component. If the MV PSP component exists on the input signal, this bit must be enabled for the MV Detection Status of register $0E_H$ to be updated.	0_B
5-3	MV PSP Detection Count	Defines the number of extra sync pulses required before declaring the Pseudo Sync Pulse (PSP) component in the MV Detection Status of register $0E_H$. The PSP component must also be present for the number of fields defined in bits 2-0 below.	100_B
2-0	MV Detection Field Count	Defines the minimum number of fields that an MV component must be present for in order to change the MV Detection Status of register $0E_H$. Add 2 to bits 2-0 to obtain the minimum field count. Ex: The default of 110_B is actually 6 + 2 = 8 fields.	110_B

TABLE 62. RESERVED

SUB ADDRESS = 42_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Reserved	Set bits 5-4 to 11_B for optimum performance.	00_H (Use 30_H)

TABLE 63. PROGRAMMABLE FRACTIONAL GAIN

SUB ADDRESS = 50_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-6	Reserved	Set to 00_B for proper operation.	00_B
5	Select PFG Enable	Set to “1” to enable the recommended PFG value in bits 4-0 below.	0_B (Use 1_B)
4-0	PFG	Programmable Fractional Gain (PFG). When enabled by bit 5, changes the loop gain (response time) of the AGC logic. Slower values provide some noise immunity to input signals with poor sync/back-porch characteristics. Recommend using the slowest PFG value of 00001_B for optimum performance. (Thus the recommended 8-bit register value = 21_H). The 5-bit PFG value has a fractional representation as: 2^0. 2^{-1} 2^{-2} 2^{-3} 2^{-4} Sample PFG values: 00000_B: Gain = 0.0000 (freezes AGC at current value) 00001_B: Gain = 0.0625 (slowest AGC response time -- recommended PFG) 01100_B: Gain = 0.7500 (default) 10000_B: Gain = 1.0000 11111_B: Gain = 1.9375 (fastest AGC response time -- not recommended)	01100_B (Use 01_H)

TABLE 64. MV STRIPE GATE

SUB ADDRESS = 51_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-6	Reserved	Set to 00_B for proper operation.	00_B
5-0	MV Stripe Gate	Defines the start of the gate for MV Color Stripe detection in $4xF_{SC}$ counts. The gate should start prior to the chroma burst. Default value of 010100_B (14_H) is valid for NTSC. Recommend 100000_B (20_H) for PAL.	010100_B

TABLE 65. RESERVED

SUB ADDRESS = 52_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Reserved	Set bit 5 to “1” for optimum performance.	02_H (Use 22_H)

TABLE 66. AGC HYSTERESIS

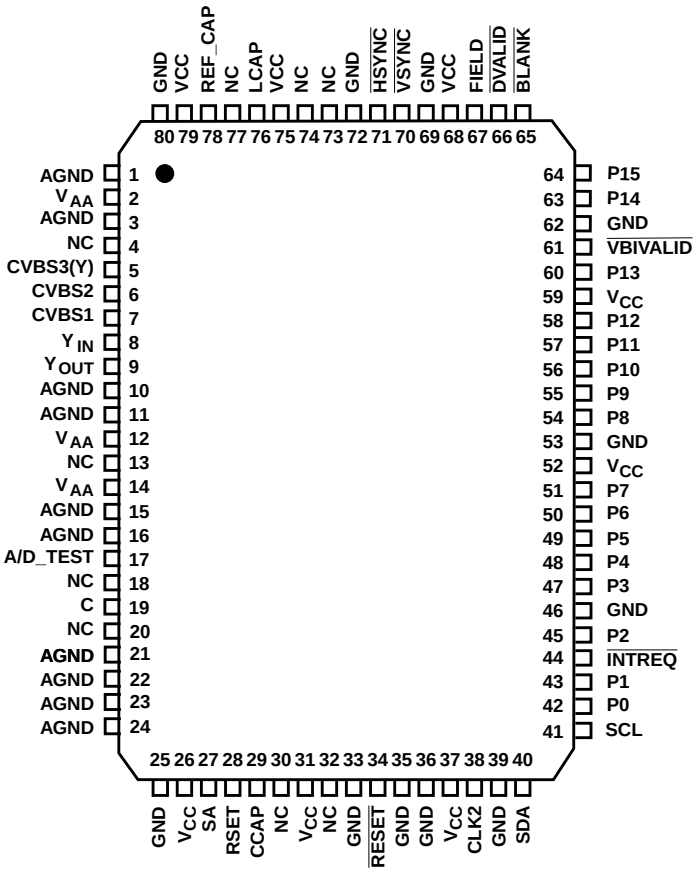
SUB ADDRESS = 53_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-4		Defines the amount of hysteresis in the AGC logic. Larger hysteresis values stabilize the AGC with poor quality input signals. For example: 0000_B = No Hysteresis 1000_B = Default Hysteresis 1111_B = Maximum Hysteresis (Recommended hysteresis value)	1000_B (Use $F0_H$)
3-0	Reserved	Set to 0000_B for proper operation.	0000_B

TABLE 67. DEVICE REVISION

SUB ADDRESS = $7F_H$			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Device Revision	This 8-bit register specifies the device revision number. Data written to this read-only register is ignored. The production baseline revision number is 01_H.	01_H

Pinout

80 LEAD PQFP
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER	I/O	PASSIVE	DESCRIPTION
CVBS1, CVBS2, CVBS3(Y)	7, 6, 5	I	75Ω Term, 1µF AC-coupled	Composite Video Inputs. CVBS3(Y) is the Luminance (Y) signal in S-Video mode. These inputs must each be terminated by a 75Ω resistor to AGND and AC-coupled by a 1.0µF capacitor as shown in the Reference Schematic. These components should be as close to this pin as possible for best performance. If not used, this pin should be connected to AGND through a 0.1µF capacitor.
YOUT	9	O	External Anti-Alias Filter	Analog output of the video multiplexer. A external low-pass anti-alias filter between the YOUT and YIN pins, as shown in the Reference Schematic. The filter components should be as close as possible to the YOUT and YIN pins for best performance.
YIN	8	I		Analog input to the ADC. See YOUT description above.
C	19	I	75Ω Term, 1µF AC-coupled and External Anti-Alias Filter	Chrominance (C) S-Video input. This input must each be terminated by a 75Ω resistor to AGND and AC-coupled by a 1.0µF capacitor as shown in the Reference Schematic. These components, and the corresponding anti-alias low-pass filter, should be as close to this pin as possible for best performance. If not used, this pin should be connected to AGND through a 0.1µF capacitor.
A/D TEST	17	O	none	Chroma signal A/D test pin. This pin must be left floating for proper operation.
RSET	28	O	12.1KΩ to AGND	A 12.1KΩ resistor must be connected between this pin and AGND. This resistor should be as close to this pin as possible for best performance. The function of this pin has changed from the HMP8112A/15 GAIN_CNTRL input. Do not use capacitor decoupling for this output pin.
REF_CAP	78	O	1.0 F to AGND	Voltage reference capacitor. A 1 F ceramic capacitor must be connected between this pin and AGND. This capacitor should be as close to this pin as possible for best performance.

Pin Descriptions (Continued)

PIN NAME	PIN NUMBER	I/O	PASSIVE	DESCRIPTION
LCAP	76	I	0.1 F to AGND	Storage capacitor for Luminance signal DC restoration. The LCAP voltage offsets the sync tip to the lower reference of the A/D. A 0.1µF capacitor should be connected between this pin and AGND. This capacitor should be as close to this pin as possible for best performance.
CCAP	29	I	0.1 F to AGND	Storage capacitor for Chrominance signal DC restoration. The CCAP voltage offsets the chroma signal to mid-range of the A/D. A 0.1µF capacitor should be connected between this pin and AGND. This capacitor should be as close to this pin as possible for best performance.
P0-P15	42, 43, 45, 47-51, 54-58, 60, 63, 64	O	N/A	Pixel output pins. See Table 3. These pins are three-stated after a $\overline{\text{RESET}}$ or software reset.
$\overline{\text{HSYNC}}$	71	O	10KΩ Pullup	Horizontal sync output. $\overline{\text{HSYNC}}$ is asserted during the horizontal sync intervals. The polarity of $\overline{\text{HSYNC}}$ is programmable. This pin is three-stated after a $\overline{\text{RESET}}$ or software reset and should be pulled high through a 10KΩ resistor.
$\overline{\text{VSYNC}}$	70	O	10KΩ Pullup	Vertical sync output. $\overline{\text{VSYNC}}$ is asserted during the vertical sync intervals. The polarity of $\overline{\text{VSYNC}}$ is programmable. This pin is three-stated after a $\overline{\text{RESET}}$ or software reset and should be pulled high through a 10KΩ resistor.
FIELD	67	O	10KΩ Pullup	FIELD output. The polarity of FIELD is programmable. This pin is three-stated after a $\overline{\text{RESET}}$ or software reset and should be pulled high through a 10KΩ resistor.
$\overline{\text{DVALID}}$	66	O	10KΩ Pullup	Data valid output. $\overline{\text{DVALID}}$ is asserted during CLK2 cycles that contain valid pixel data. This pin is three-stated after a $\overline{\text{RESET}}$ or software reset and should be pulled high through a 10KΩ resistor.
$\overline{\text{BLANK}}$	65	O	10KΩ Pullup	Composite blanking output. $\overline{\text{BLANK}}$ is asserted during the horizontal and vertical blanking intervals. The polarity of $\overline{\text{BLANK}}$ is programmable. This pin is three-stated after a $\overline{\text{RESET}}$ or software reset and should be pulled high through a 10KΩ resistor.
$\overline{\text{VBIVALID}}$	61	O	10KΩ Pullup	Vertical Blanking Interval Valid output. $\overline{\text{VBIVALID}}$ is asserted during CLK2 cycles that contain valid VBI (Vertical Blanking Interval) data such as Closed Captioning, Teletext, and WSS data. The polarity of $\overline{\text{VBIVALID}}$ is programmable. This pin is three-stated after a $\overline{\text{RESET}}$ or software reset and should be pulled high through a 10K resistor.
$\overline{\text{INTREQ}}$	44	O	10KΩ Pullup	Interrupt Request Output. This is an open-drain output and requires an external 10KΩ pull-up resistor to V_{CC}.
CLK2	38	I		2x pixel clock input. This clock must be a continuous, free-running clock. Refer to Table 1 for allowable CLK2 frequencies for each video standard and aspect ratio. For best performance, use termination resistor(s) to minimize pulse overshoot and reflections.
$\overline{\text{RESET}}$	34	I		Reset control input. A logical zero for a minimum of four CLK2 cycles resets the device. $\overline{\text{RESET}}$ must be a logical one for normal operation.
SA	27	I	10KΩ Pullup or 0Ω Pulldown	I^2C slave address select input. This was formerly the WPE pin on HMP8112/15 decoders. If the SA pin is pulled low, the I^2C address is 1000100xB or 88_H. If the SA pin is pulled high, the address is 1000101xB or $8A_H$. (The 'x' bit is the address is the I2C read flag.)
SDA	40	I/O	4KΩ Pullup	I^2C data input/output. This pin should be pulled high through a 4KΩ resistor.
SCL	41	I	4KΩ Pullup	I^2C clock input. This pin should be pulled high through a 4KΩ resistor.
VAA	2, 12, 14	I	0.1 F to AGND	Analog power supply pins. All VAA pins must be connected together.
AGND	1, 3, 10, 11, 15,16, 21, 22, 23, 24	I	none	Analog ground pins. All AGND pins must be connected together. Refer to Applications section for recommended grounding scheme.
VCC	26, 31,37, 52, 59, 68, 75, 79	I		Digital power supply pins. All VCC pins must be connected together.
GND	25, 33, 35, 36, 39, 46, 53, 62, 69, 72, 80	I		Digital ground pins. All GND pins must be connected together.
NC	4, 13, 18, 20, 30, 32, 73, 74, 77			No Connect pins. These pins may be left floating or tied to GND.

Applications Information

Direct Interface to Video Encoders

Direct interface to a video encoder will induce pixel jitter in the output video and is therefore not recommended as a primary data interface. The jitter will occur with all decoder output formats, including BT.656. However, pixel jitter may be acceptable for some applications; such as a “preview mode” prior to image capture or compression. For more detail, reference “CYCLE SLIPPING AND REAL-TIME PIXEL JITTER” section from this data sheet.

Decoder Upgrades

The following table describe the impacts to pins for upgrading from the HMP8112/A or HMP8115 to the HMP8117.

TABLE 68. UPGRADING FROM HMP8112/A OR HMP8115

Pin #	HMP8112/15 Pin	HMP8117 Impact
28	GAIN_CNTL (Now RSET)	Use single 12.1K resistor to AGND. Remove any decoupling caps.
78	DEC_T (Now REF_CAP)	Change to single 1.0uF capacitor (1206-size XR7-type) to AGND.
29	CCLAMP_CAP (Now CCAP)	Change to 0.1uF capacitor.
76	LCLAMP_CAP (Now LCAP)	Change to 0.1uF capacitor.
9,8,19	L_OUT, L_ADIN, and C	Recommend use of new anti-alias filter from Reference Schematic.
27	WPE (Now SA)	Pull low for I2C address compatibility with HMP8112/A.
44	DVCC/NC (Now $\overline{\text{INTREQ}}$)	Pin actually NC on HMP8112/A. Float or use 10K pullup to VCC.
61	DGND/NC (Now $\overline{\text{VBIVALID}}$)	Pin actually NC on HMP8112/A. Float or use 10K pullup to VCC.
13	CLK2 (Now NC)	Trace may be deleted to reduce reflections on CLK2 at pin 38.
30, 32, 73, 77	DEC_L, DGND, DGND, AGC_CAP	Pins no longer used (NC). Capacitors used at these pins may be removed.

Typical Programming Sequence

The following pseudo code provides a typical programming sequence to initialize the HMP8117 using the default 16-bit YCbCr output data format.

```
SetReg 0x1F = 0x80 // Soft Reset
SetReg 0x37 = 0x90 // Wider HSYNC Detect Window
SetReg 0x42 = 0x30 // Recommended Value
SetReg 0x50 = 0x21 // Slower PFG
SetReg 0x52 = 0x22 // Recommended Value
SetReg 0x53 = 0xF0 // Large AGC Hysteresis
SetReg 0x03 = 0xC0 // Enable Data/Timing Outputs
```

PCB Layout Considerations

A PCB board with a minimum of 4 layers is recommended, with layers 1 and 4 (top and bottom) for signals and layers 2 and 3 for power and ground. The PCB layout should implement the lowest possible noise on the power and ground planes by providing excellent decoupling. The optimum layout places the HMP8117 as close as possible to the power supply connector and the video input connector. Place external components as close as possible to the appropriate pin using short, wide traces.

ANALOG POWER PLANE

The analog power plane (V_{AA}) is recommended to be separate from the common board digital power plane (V_{CC}) with a gap between the two planes of at least 1/8 inch. The V_{AA} plane should be connected to the V_{CC} plane at a single point though a low-resistance ferrite bead, such as a Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001. The ferrite bead provides resistance to switching currents, improving the performance of HMP8117.

If a separate linear regulator is used to provide power to the analog power plane, the power-up sequence should be designed to ensure latch up will not occur. A separate linear regulator is recommended if the power supply noise on the V_{AA} pins exceeds 200mV.

ANALOG GROUND PLANE

A separate analog ground (AGND) plane is recommended with a single point connection to the digital ground (GND) plane using a ferrite bead as mentioned above.

POWER SUPPLY DECOUPLING

Decouple each V_{AA} and V_{CC} pin to the appropriate ground plane using a 0.1µF ceramic chip capacitor. Bulk decouple the power planes using a 1.0µF ceramic chip capacitor located at each corner of the device. (One capacitor placed at the top left corner for V_{AA} and three capacitors placed at the other corners for V_{CC}.) A single 47µF decoupling capacitor for the analog power plane may also be used to control excessive low-frequency power supply ripple. See Figure 20, HMP8117 Reference Schematics.

ANALOG SIGNALS

Traces containing digital signals should not be routed over, under, or adjacent to the analog output traces to minimize cross-talk. If this is not possible, coupling can be minimized by routing the digital signals at a 90 degree angle to the analog signals. The analog traces should also not overlay the V_{CC} power plane to maximize high-frequency power supply rejection.

Evaluation Board

HMPVIDEVAL/ISA

The HMPVIDEVAL/ISA board provides a complete video frame-grabber platform to evaluate all modes of the video decoder and encoder. The ISA style PC add-in board supports a complete Windows 95 software application to easily operate all features of the evaluation platform.

Related Application Notes

Application Notes are also available on the Intersil Multimedia web site at http://www.intersil.com/mmedia.

AN9644: Composite Video Separation Techniques

AN9716: Wide Screen Signalling

AN9717: YCbCr to RGB Considerations

AN9728: BT.656 Video Interface for ICs

AN9806: Advantages of the HMP8117 Videolyzer Operation

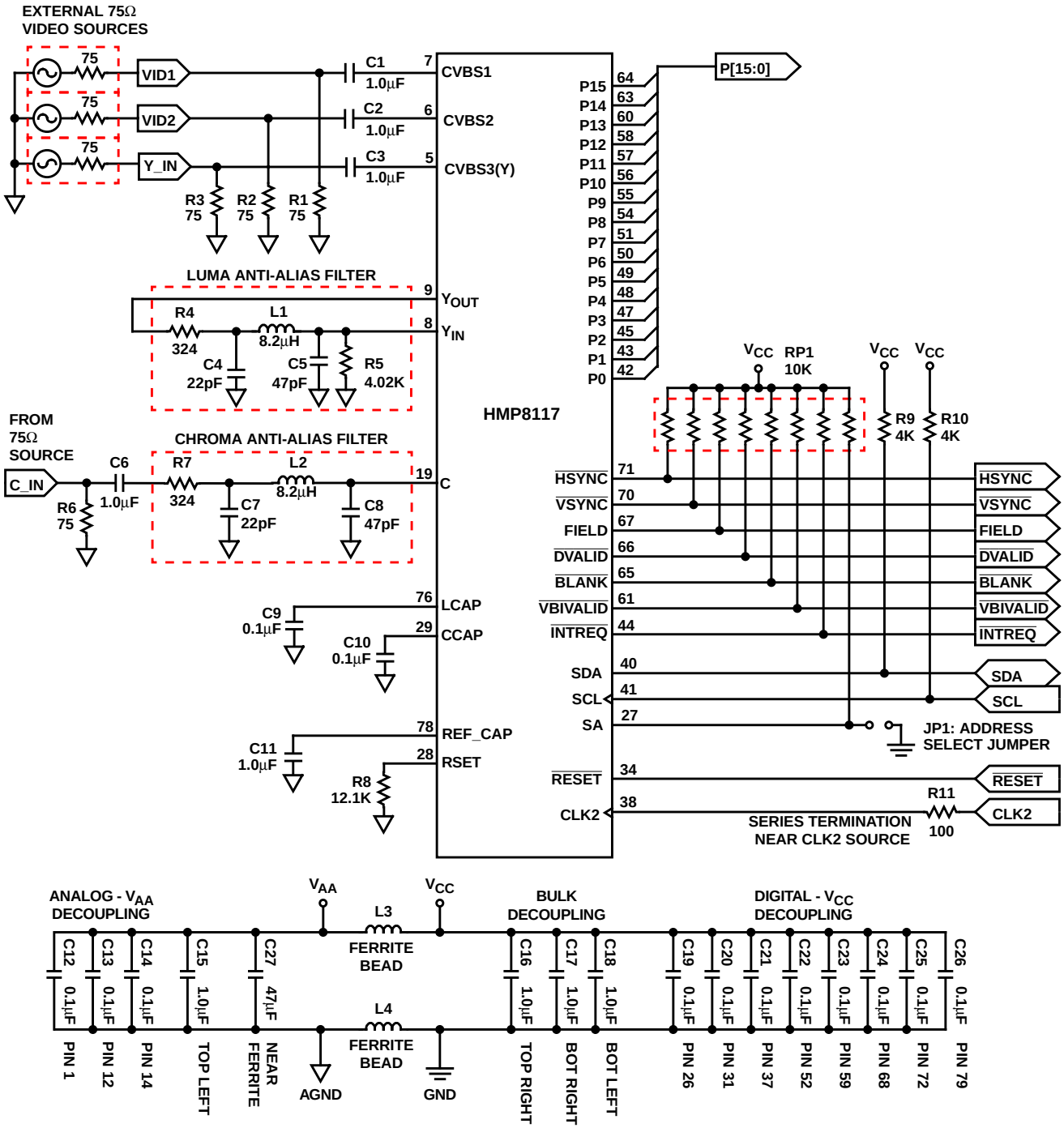


FIGURE 20. HMP8117 REFERENCE SCHEMATICS

Absolute Maximum Ratings

Digital Supply Voltage (V_{CC} to GND) 7.0V
Analog Supply Voltage (VAA to GND) 7.0V
Digital Input Voltages . . . . . GND - 0.5V to V_{CC} + 0.5V
ESD Classification . . . . . Class 1

Operating Temperature Range

HMP8117CN . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, See Note 40) θ_{JA} ($^oC/W$)
MQFP Package 45
Maximum Power Dissipation
HMP8117CN 1.78W
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Junction Temperatures . . . . . 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

40. θ_{JA} is measured with the component mounted on an evaluation PC board in free air. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Electrical Specifications $V_{CC} = V_{AA} = 5.0V, T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
POWER SUPPLY CHARACTERISTICS						
Power Supply Voltage Range	V_{CC}, V_{AA}	(Note 2)	4.75	5	5.25	V
Total Power Supply Current	I_{TOT}	CLK2 = 29.5MHz, V_{CC} = VAA = 5.25V Outputs Not Loaded	-	279	305	mA
Digital Power Supply Current	I_{CC}		-	132	-	mA
Analog Power Supply Current	I_{AA}		-	147	-	mA
Total Power Dissipation	P_{TOT}		-	1.46	1.60	W
DC CHARACTERISTICS: DIGITAL I/O (EXCEPT CLK2 and I^2C INTERFACE)						
Input Logic High Voltage	V_{IH}	V_{CC} = Max	2.0	-	-	V
Input Logic Low Voltage	V_{IL}	V_{CC} = Min	-	-	0.8	V
Output Logic High Voltage	V_{OH}	I_{OH} = -4mA, V_{CC} = Max	2.4	-	-	V
Output Logic Low Voltage	V_{OL}	I_{OL} = 4mA, V_{CC} = Min	-	-	0.4	V
Input Leakage Current	I_{IH}, I_{IL}	V_{CC} = Max, Input = 0V or 5V	-10	-	10	µA
Input/Output Capacitance	C_{IN}, C_{OUT}	f = 1MHz (Note 2) All Measurements Referenced to Ground, $T_A = 25^oC$	-	8	-	pF
Three-State Output Current Leakage	I_{OZ}		-10	-	10	µA
DC CHARACTERISTICS: CLK2 DIGITAL INPUT						
Input Logic High Voltage	V_{IH}	V_{CC} = Max	$0.7xV_{CC}$	-	-	V
Input Logic Low Voltage	V_{IL}	V_{CC} = Min	-	-	$0.3xV_{CC}$	V
Input Leakage Current	I_{IH}	V_{CC} = Max Input = 0V or V_{CC}	-10	-	10	µA
	I_{IL}		- 450	-	-	µA
Input Capacitance	C_{IN}	CLK2 = 1MHz (Note 2) All Measurements Referenced to Ground, $T_A = 25^oC$	-	8	-	pF
DC CHARACTERISTICS: I^2C INTERFACE						
Input Logic High Voltage	V_{IH}	V_{CC} = Max	$0.7xV_{CC}$	-	-	V
Input Logic Low Voltage	V_{IL}	V_{CC} = Min	-	-	$0.3xV_{CC}$	V
Output Logic High Voltage	V_{OH}	I_{OH} = -1mA, V_{CC} = Max	3.0	-	-	V
Output Logic Low Voltage	V_{OL}	I_{OL} = 3mA, V_{CC} = Min	0	-	0.4	V

Electrical Specifications $V_{CC} = V_{AA} = 5.0V$, $T_A = 25^oC$ **(Continued)**

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IH}, I_{IL}	V_{CC} = Max, Input = 0V or 5V	-	-	10	µA
Input/Output Capacitance	C_{IN}, C_{OUT}	SCL = 400kHz, (Note 2) All Measurements Referenced to GND, $T_A = 25^oC$	-	8	-	pF
AC CHARACTERISTICS: DIGITAL I/O (EXCEPT I^2C INTERFACE)						
CLK2 Frequency			24.54	-	29.5	MHz
CLK2 Waveform Symmetry		(Note 2)	40	-	60	%
CLK2 Pulse Width High	t_{PWH}		13	-	-	ns
CLK2 Pulse Width Low	t_{PWL}		13	-	-	ns
Data and Control Setup Time	t_{SU}	(Note 3)	10	-	-	ns
Data and Control Hold Time	t_{HD}		0	-	-	ns
CLK2 to Output Delay	t_{DVLD}		0	-	23	ns
Data and Control Rise/Fall Time	t_r, t_f	(Note 2)	1	-	12	ns
AC CHARACTERISTICS: I^2C INTERFACE						
SCL Clock Frequency	f_{SCL}		0	-	400	kHz
SCL Pulse Width Low	t_{LOW}		1.3	-	-	µs
SCL Pulse Width High	t_{HIGH}		0.6	-	-	µs
Data Hold Time	$t_{HD:DATA}$		0	-	-	ns
Data Setup Time	$t_{SU:DATA}$		100	-	-	ns
SDA, SCL Rise Time	t_R	(Note 2)	-	-	300	ns
SDA, SCL Fall Time	t_F		-	-	300	ns
ANALOG INPUT PERFORMANCE						
Composite Video Input Amplitude (Sync Tip to White Level)		Input Termination of 75Ω and 1.0µF AC-Coupled	0.5	1.0	2.0	V_{P-P}
Luminance (Y) Video Input Amplitude (Sync Tip to White Level)		Input Termination of 75Ω and 1.0µF AC-Coupled	0.5	1.0	2.0	V_{P-P}
Chrominance (C) Video Input Amplitude (Burst Amplitude)		Input Termination of 75Ω and 1.0µF AC-Coupled, (Note 2)	0.143	0.286	0.6	V_{P-P}
Video Input Impedance	R_{AIN}	(Note 2)	200	-	-	kΩ
Video Input Bandwidth	BW	$1V_{P-P}$ Sine Wave Input to -3dBc Reduction, (Note 2)	5	-	-	MHz
ADC Input Range	A_{IN} FULL SCALE		-	1	-	V_{P-P}
	A_{IN} OFFSET		-	1.5	-	V
ADC Integral Nonlinearity	INL	Best Fit Linearity	-	± 2	-	LSB
ADC Differential Nonlinearity	DNL		-	± 0.35	-	LSB
VIDEO PERFORMANCE						
Differential Gain	DG	Modulated Ramp (Note 2)	-	2	-	%
Differential Phase	DP		-	1	-	Deg.
Hue Accuracy		75% Color Bars (Note 2)	-	2	-	Deg.
Color Saturation Accuracy			-	2	-	%
Luminance Nonlinearity		NTC-7 Composite (Note 2)	-	2	-	%
SNR	$SNRL_{WEIGHTED}$	Pedestal Input (Note 2)	-	50	-	dB

Electrical Specifications $V_{CC} = V_{AA} = 5.0V, T_A = 25^oC$ **(Continued)**

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
GENLOCK PERFORMANCE						
Horizontal Locking Time	t_{LOCK}	Time from Initial Lock Acquisition to an Error of 1 Pixel. (Note 2)	2	3	-	Fields
Long-Term horizontal Sync Lock Range		Range over specified pixel jitter is maintained. Assumes line time changes by amount indicated slowly between over one field. (Note 2)	-	-	5	%
Number of Missing Horizontal Syncs Before Lost Lock Declared	$H_{SYNC\ LOST}$	Programmable via register 04_H (Note 2)	1 or 12	1 or 12	1 or 12	HSYNCs
Number of Missing Vertical Syncs Before Lost Lock Declared	$V_{SYNC\ LOST}$		1 or 3	1 or 3	1 or 3	VSYNCs
Long-Term Color Subcarrier Lock Range		Range over color subcarrier locking time and accuracy specifications are maintained. Subcarrier frequency changes by amount indicated slowly over 24 hours. (Note 2)	-	±200	±400	Hz
Vertical Sample Alignment		(Notes 2, 4)	-	1/8	-	Pixel
			-	10	-	ns

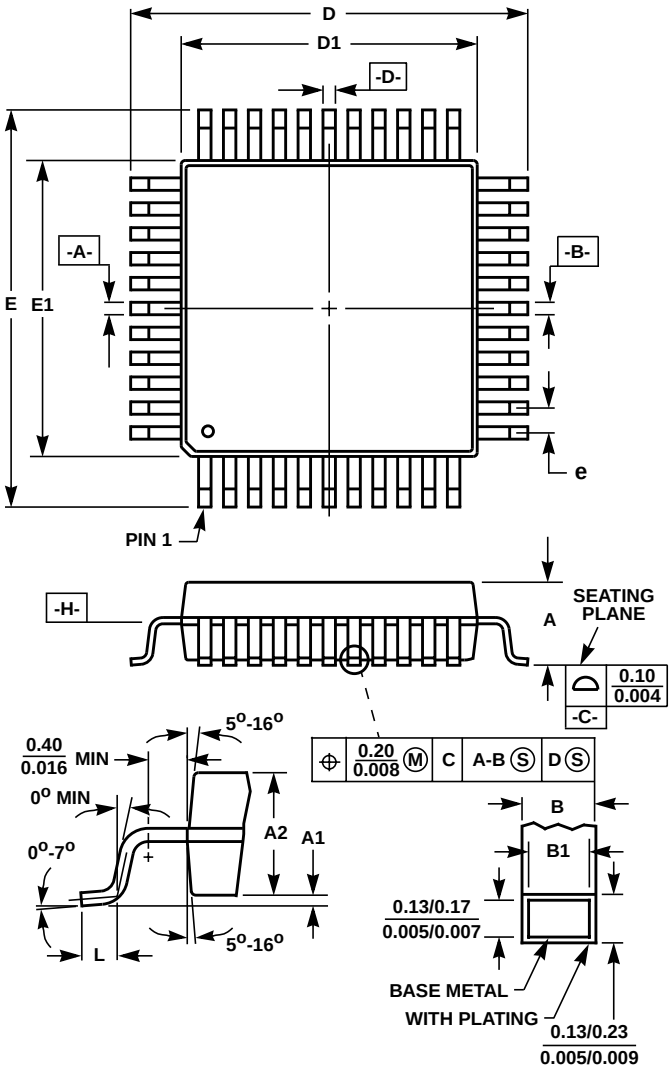
NOTES:

41. Guaranteed by design or characterization.

42. Test performed with $C_L = 40pF$, $I_{OL} = 4mA$, $I_{OH} = -4mA$. Input reference level is 1.5V for all inputs. $V_{IH} = 3.0V$, $V_{IL} = 0V$.

43. Since the HMP8117 does not generate the sample clock, any clock jitter present on the CLK2 input will directly translate to pixel jitter on the output data. The Vertical Sample Alignment parameter specifies the spatial pixel alignment from one scan line to the next using a stable CLK2 source.

Metric Plastic Quad Flatpack Packages (MQFP/PQFP)



Q80.14x20 (JEDEC MO-108CB-1 ISSUE A)
80 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.134	-	3.40	-
A1	0.010	-	0.25	-	-
A2	0.100	0.120	2.55	3.05	-
B	0.012	0.018	0.30	0.45	6
B1	0.012	0.016	0.30	0.40	-
D	0.904	0.923	22.95	23.45	3
D1	0.783	0.791	19.90	20.10	4, 5
E	0.667	0.687	16.95	17.45	3
E1	0.547	0.555	13.90	14.10	4, 5
L	0.026	0.037	0.65	0.95	-
N	80		80		7
e	0.032 BSC		0.80 BSC		-
ND	24		24		-
NE	16		16		-

Rev. 0 1/94

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. “N” is the number of terminal positions.

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029