FAIRCHILD SEMICONDUCTOR™

July 1988
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100351
Low Power Hex D-Type Flip-Flop

General Description

The 100351 contains six D-type edge-triggered, master/slave flip-flops with true and complement outputs, a pair of common Clock inputs (CP_a and CP_b) and common Master Reset (MR) input. Data enters a master when both CP_a and CP_b are LOW and transfers to the slave when CP_a and CP_b (or both) go HIGH. The MR input overrides all other inputs and makes the Q outputs LOW. All inputs have 50 kΩ pull-down resistors.

Features

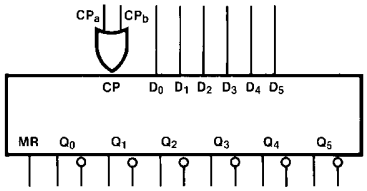
- 40% power reduction of the 100151
- 2000V ESD protection
- Pin/function compatible with 100151
- Voltage compensated operating range: –4.2V to –5.7V
- Available to industrial grade temperature range

Ordering Code:

Order Number	Package Number	Package Description
100351SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
100351PC	N24E	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
100351QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
100351QI	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Industrial Temperature Range (–40°C to +85°C)

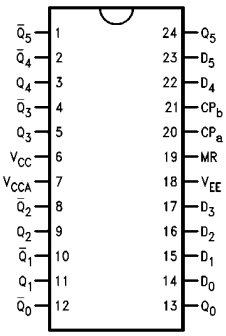
Devises also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol

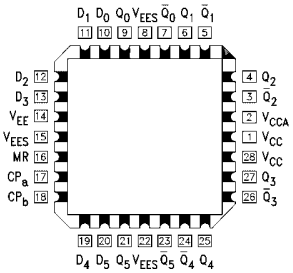


Connection Diagrams

24-Pin DIP/SOIC



28-Pin PLCC



Pin Descriptions

Pin Names	Description
D_0–D_5	Data Inputs
CP_a, CP_b	Common Clock Inputs
MR	Asynchronous Master Reset Input
Q_0–Q_5	Data Outputs
$\overline{Q}_0$–$\overline{Q}_5$	Complementary Data Outputs

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Truth Tables

(Each Flip-flop)

Synchronous Operation

Inputs				Outputs
D_n	CP_a	CP_b	MR	$Q_n(t+1)$
L	⌐	L	L	L
H	⌐	L	L	H
L	L	⌐	L	L
H	L	⌐	L	H
X	H	⌐	L	$Q_n(t)$
X	⌐	H	L	$Q_n(t)$
X	L	L	L	$Q_n(t)$

Asynchronous Operation

Inputs				Outputs
D_n	CP_a	CP_b	MR	$Q_n(t+1)$
X	X	X	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

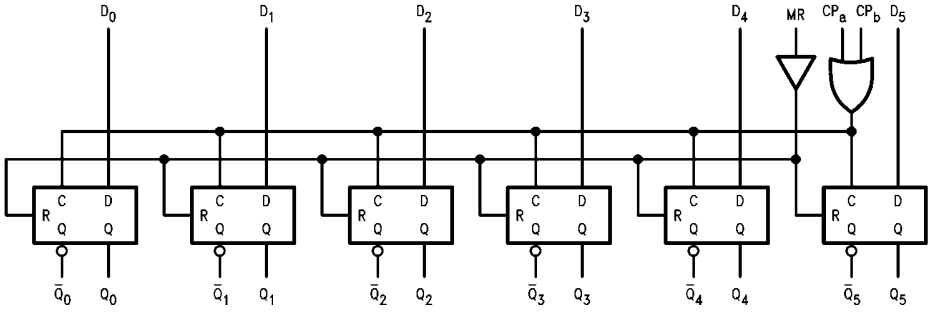
X = Don't Care

t = Time before CP positive transition

t+1 = Time after CP positive transition

⌐ = LOW-to-HIGH transition

Logic Diagram



Absolute Maximum Ratings(Note 1)

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Commercial Version

DC Electrical Characteristics (Note 3)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max)	Loading with
V_{OL}	Output LOW Voltage	−1830	−1705	−1620		or V_{IL} (Min)	50Ω to −2.0V
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min)	Loading with
V_{OLC}	Output LOW Voltage			−1610		or V_{IL} (Max)	50Ω to −2.0V
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			µA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current						
	MR			350	µA	V_{IN} = V_{IH} (Max)	
	D_0–D_5			240			
	CP_a, CP_b			350			
I_{EE}	Power Supply Current	−129		−62	mA	Inputs OPEN	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{MAX}	Toggle Frequency	375		375		375		MHz	Figures 2, 3
t_{PLH}	Propagation Delay	0.80	2.00	0.80	2.0	0.90	2.10	ns	Figures 1, 3
t_{PHL}	CP_a, CP_b to Output								
t_{PLH}	Propagation Delay	1.10	2.30	1.10	2.30	1.20	2.40	ns	Figures 1, 4
t_{PHL}	MR to Output								
t_{TLH}	Transition Time	0.35	1.20	0.35	1.20	0.35	1.20	ns	Figures 1, 3
t_{THL}	20% to 80%, 80% to 20%								
t_S	Setup Time								
	D_0–D_5	0.40		0.40		0.40		ns	Figure 5
	MR (Release Time)	1.60		1.60		1.60			Figure 4
t_H	Hold Time	0.80		0.80		0.80		ns	Figure 5
	D_0–D_5								
t_{PW}(H)	Pulse Width HIGH	2.00		2.00		2.00		ns	Figures 3, 4
	CP_a, CP_b, MR								

Commercial Version (Continued)
SOIC and PLCC AC Electrical Characteristics

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{MAX}	Toggle Frequency	375		375		375		MHz	Figures 2, 3
t_{PLH} t_{PHL}	Propagation Delay CP_a, CP_b to Output	0.80	1.80	0.80	1.80	0.90	1.90	ns	Figures 1, 3
t_{PLH} t_{PHL}	Propagation Delay MR to Output	1.10	2.10	1.10	2.10	1.20	2.20	ns	Figures 1, 4
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.60	0.45	1.70	ns	Figures 1, 3
t_S	Setup Time D_0–D_5	0.30		0.30		0.30		ns	Figure 5
	MR (Release Time)	1.50		1.50		1.50			Figure 4
t_H	Hold Time D_0–D_5	0.80		0.80		0.80		ns	Figure 5
t_{PW}(H)	Pulse Width HIGH CP_a, CP_b, MR	2.00		2.00		2.00		ns	Figures 3, 4
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path		220		220		220	ps	PLCC only (Note 4)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path		210		210		210	ps	PLCC only (Note 4)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Clock to Output Path		240		240		240	ps	PLCC only (Note 4)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Clock to Output Path		230		230		230	ps	PLCC only (Note 4)

Note 4: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}), or LOW-to-HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Industrial Version

PLCC DC Electrical Characteristics

V_{EE}=–4.2V to –5.7V, V_{CC}=V_{CCA}= GND, T_C= 0°C to +85°C (Note 5)

Symbol	Parameter	T_C = –40°C		T_C = 0° to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	–1085	–870	–1025	–870	mV	V_{IN} =V_{IH} (Max)	Loading with
V_{OL}	Output LOW Voltage	–1830	–1575	–1830	–1620		or V_{IL} (Min)	50Ω to –2.0V
V_{OHC}	Output HIGH Voltage	–1095		–1035		mV	V_{IN} = V_{IH} (Min)	Loading with
V_{OLC}	Output LOW Voltage		–1565		–1610		or V_{IL} (Max)	50Ω to –2.0V
V_{IH}	Input HIGH Voltage	–1170	–870	–1165	–870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	–1830	–1480	–1830	–1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		µA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current							
	MR		350		350			
	D_0–D_5		240		240	µA	V_{IN} = V_{IH} (Max)	
	CP_a, CP_b		350		350			
I_{EE}	Power Supply Current	–129	–62	–129	–62	mA	Inputs OPEN	

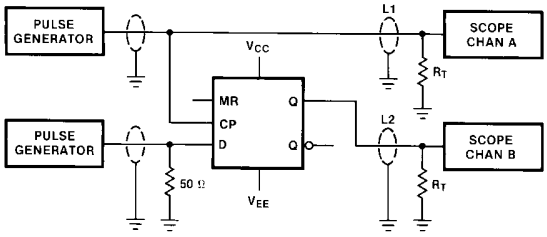
Note 5: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PLCC AC Electrical Characteristics

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = –40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{MAX}	Toggle Frequency	375		375		375		MHz	Figures 2, 3
t_{PLH} t_{PHL}	Propagation Delay CP_a, CP_b to Output	0.80	1.80	0.80	1.80	0.90	1.90	ns	Figures 1, 3
t_{PLH} t_{PHL}	Propagation Delay MR to Output	1.10	2.10	1.10	2.10	1.20	2.20	ns	Figures 1, 4
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.60	0.45	1.70	ns	Figures 1, 3
t_S	Setup Time								
	D_0–D_5	0.60		0.30		0.30		ns	Figure 5
	MR (Release Time)	2.20		1.50		1.50			Figure 4
t_H	Hold Time D_0–D_5	0.60		0.90		0.90		ns	Figure 5
t_{PW}(H)	Pulse Width HIGH CP_a, CP_b, MR	2.00		2.00		2.00		ns	Figures 3, 4

Test Circuitry



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance lines

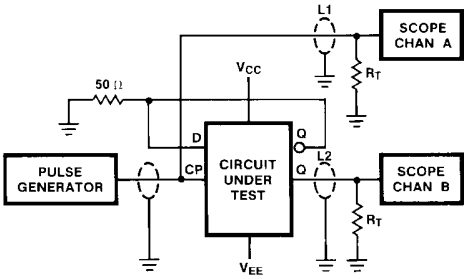
R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Jig and stray capacitance ≤ 3 pF

FIGURE 2. Toggle Frequency Test Circuit

Switching Waveforms

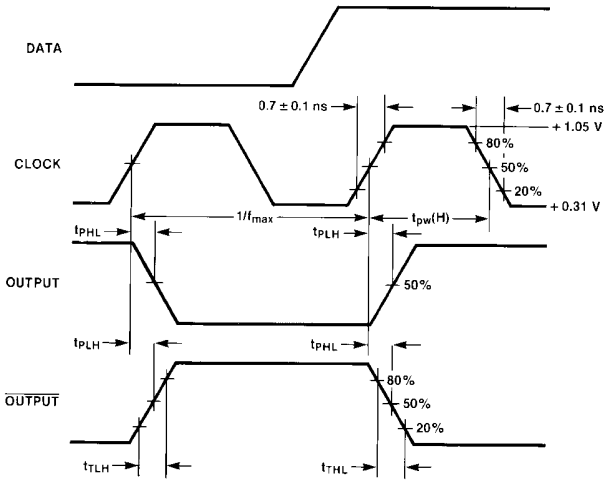


FIGURE 3. Propagation Delay (Clock) and Transition Times

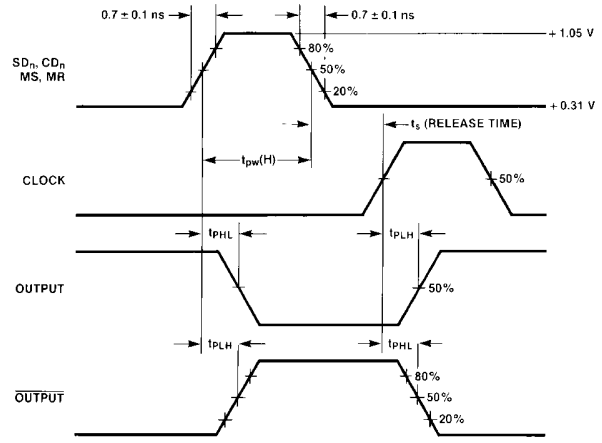
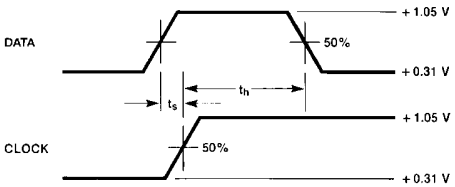


FIGURE 4. Propagation Delay (Reset)



Notes:

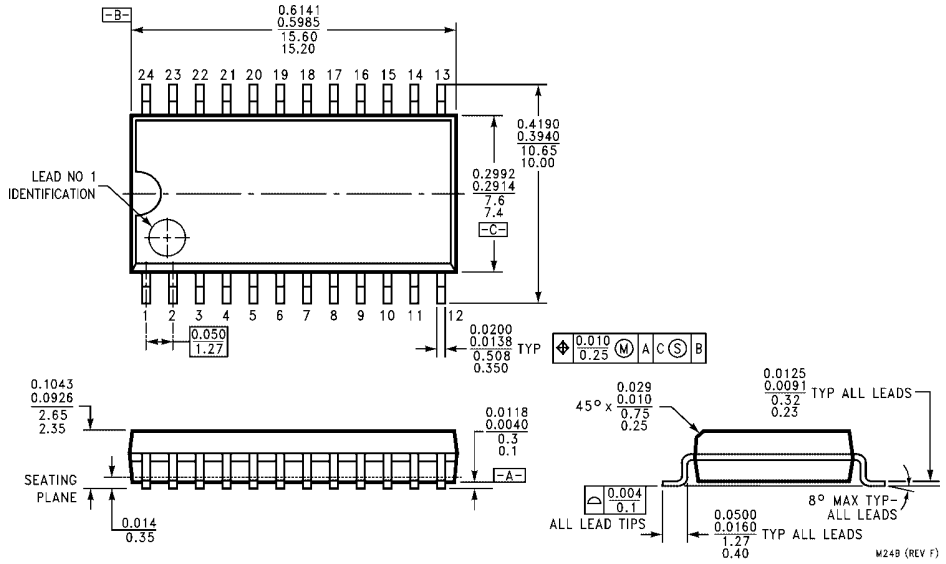
t_S is the minimum time before the transition of the clock that information must be present at the data input.

t_H is the minimum time after the transition of the clock that information must remain unchanged at the data input.

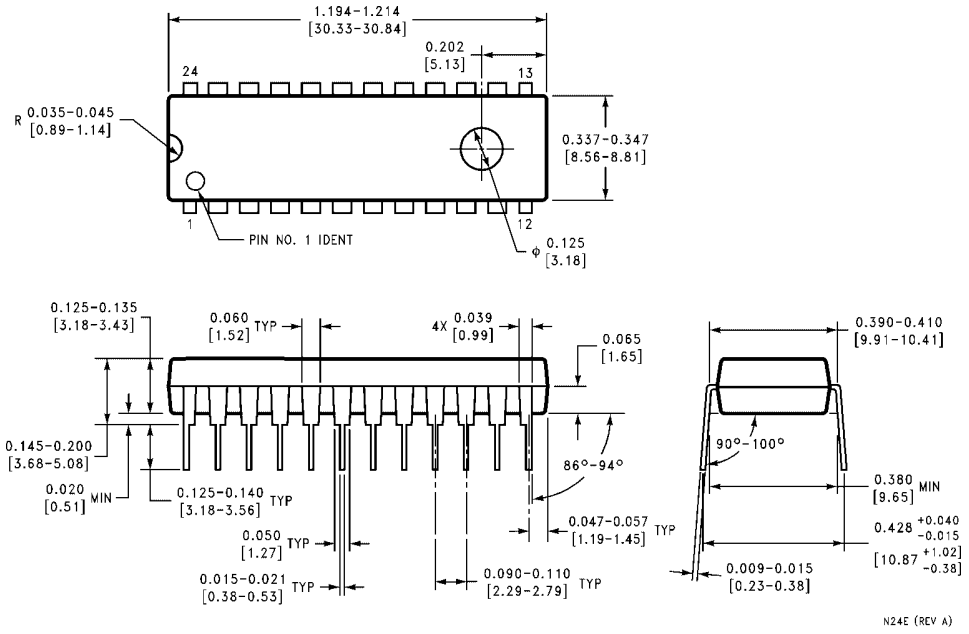
FIGURE 5. Setup and Hold Time

100351

Physical Dimensions inches (millimeters) unless otherwise noted

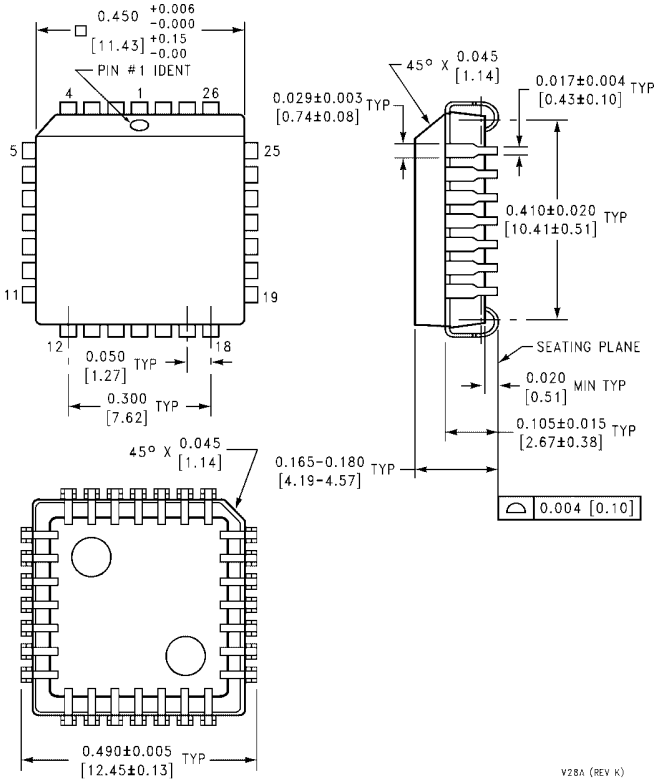


24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
Package Number N24E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
Package Number V28A

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